APF® Pitch-Halving for 22nm Logic Cells using Gridded Design Rules

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ABSTRACT

The 22nm logic technology node with dimensions of ~32nm will be the first node to require some form of pitch-halving. A unique combination of a Producer APF®-based process sequence and GDR-based design style permits implementation of random logic functions with regular layout patterns. The APF (Advanced Patterning Film) pitch-halving approach is a classic Self-Aligned Double Patterning scheme (SADP) [1,2,3,4] which involves the creation of CVD dielectric spacers on an APF sacrificial template and using the spacers as a hardmask for line frequency doubling. The Tela Canvas™ implements Gridded Design Rules (GDR) using straight lines placed on a regular grid. Logic functions can be implemented using lines on a half-pitch with gaps at selected locations.

Keywords: APF, Advanced Patterning Film, GDR, Gridded Design Rules, restricted design rules, double patterning, spacer mask, SADP, SaDPT

1. INTRODUCTION

Scaling of integrated circuits over the past 50 years has been enabled by the dramatic improvements in overlay and resolution of photolithography equipment. During this time, equipment cost increases have been offset by increased productivity, keeping the final products on well documented learning curves such as the price per DRAM bit (currently measured in micro-cents).

The forecast for photolithography performance needs and solutions has been coordinated by the ITRS organization for many years, with biannual updates [5]. Several technologies have come and gone from these forecasts, for example 157nm F_2 excimer laser illumination, reflecting the continual struggle to achieve technical progress at affordable costs at the right time. The 2006 update of the ITRS shows all of the lithography resolution-limited factors as yellow or red for 2008, highlighting the difficulties faced by companies trying to develop scaled technologies.

Using the Rayleigh equation, $CD = k_1 \lambda/NA$, it becomes clear that if progress is not made in the wavelength λ, or the numerical aperture NA, then the burden of scaling to smaller CD's falls to the fitting factor k_1. Given that the last optical scanner announced for production was introduced in 2007, the industry is faced with λ/NA = 143nm for the foreseeable future. The trend in CD (half-pitch) and wavelength is illustrated in Figure 1 for logic technology nodes from 180nm to 22nm. Where the curves separate, k_1 has to decrease to make up the difference.

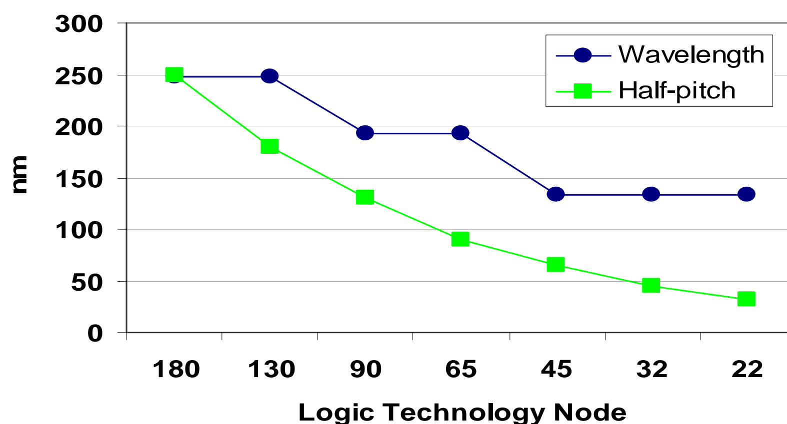

Fig. 1. Trend in illumination wavelength and feature size half-pitch for logic technology nodes.

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The 22nm logic technology node is expected to have a metal-1 half-pitch of approximately 32nm when production starts in 2013. If λ/NA = 143nm remains true for production equipment, then the required k_1 value is 0.22. This is well below the practical limits of 0.37 for 2D patterns and 0.28 for 1D patterns, and the theoretical limit of 0.25 [6].

Double patterning has been proposed as a potential solution. 193i double patterning was added to the ITRS roadmap in the 2006 update for 45nm and 32nm half-pitch technologies. There are a number of drawbacks to either double exposure or double exposure / double etch. The issues include the EDA problem of splitting the pattern correctly, OPC for semi-isolated features, overlay of the patterns on masks and subsequently wafers, cost of two immersion scanner passes, and defectivity from the additional operations. There is also the problem that most double patterning is really triple patterning, with two passes of critical line exposure and one pass of less critical end cutting.

The 22nm logic node solution studied in this paper involves pitch halving using a sequence of deposition and etching steps instead of multiple critical exposure steps. The use of APF (Advanced Patterning Film) as an easily removable hard mask is an important enabling factor. The GDR (Gridded Design Rule) design style, using the Tela Canvas™ and logic architecture, is the other key element making the structures useful for circuit design. The combination of SADP and Tela Canvas™ may be considered to extend the capability of existing wafer fabs to smaller CD's with minimal investment.

2. APF PROCESS SEQUENCE FOR PITCH HALVING

The APF based SADP sequence for pitch halving involves

- Printing at a pitch of twice the target pitch.
- Resist trimming to a 1:3 (line to space) ratio
- Etching a sacrificial template (in this case APF)
- Forming sidewall spacers of the desired final linewidth.
- Removing the original template material (in this case by O2 ash).
- Utilizing the sidewall spacers as hardmask for patterning substrate.
- Perpendicular cuts can be etched for generating circuit functions.

The creation of 22nm half-pitch GDR (gridded design rule) structures combines the prior art of (a) 22nm half-pitch SADP intended for NAND Flash array patterning [1,2] with (b) the cutting of array structures for manipulation into non-Flash circuits [3,7,8,9]. To demonstrate the most basic structure, we focused on generating 22nm patterns comprised of both long lines and small islands mixed densely together.

2.1 Forming 22nm half-pitch arrays

To create an initial 22nm line and space array, we designed a patterning film stack starting with a CVD amorphous carbon hardmask (APF), with a CVD nitride (or silicon) cap, followed by another CVD amorphous carbon to be used as a sacrificial template, with another dielectric cap. The full sequence is depicted in Figure 2. Photolithography was performed using an ASML 1700i water immersion tool, printing 45nm lines and spaces, which were subsequently trimmed to 23nm lines (67nm space) before etching the APF template. Following this, a CVD dielectric spacer was deposited targeting a 22nm sidewall width, leaving a 23nm gap between spacers. After spacer etch, the APF template was cleanly removed using a conventional oxygen ash process requiring no wet-clean. Finally, the spacers were used as a hardmask to transfer the pattern into the bottom layer of APF, which was then used to drive the final pattern into silicon. Since APF is a widely adopted hardmask for most dielectrics and conductors used in the semiconductor industry, this scheme could be applied universally to any desired substrate material. SEM image snapshots of the process flow are shown below in Figure 3. The CD performance typically obtained on small wafer runs, measuring 20 die per wafer, is in the range of 1-2nm (3 sigma) and less than 2nm (mean) for line edge and line width roughness as illustrated in Figure 4. For additional details on 22nm SADP, please refer to the accompanying conference paper (6924-169) entitled "22nm Half-Pitch Patterning by CVD Spacer Self Alignment Double Patterning (SADP)".

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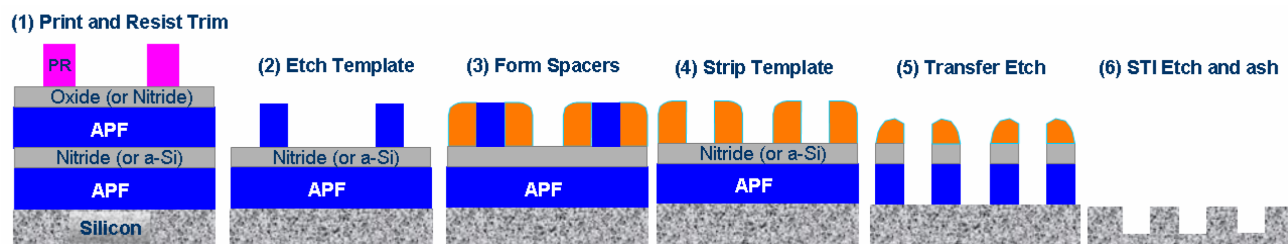


Figure 2: Illustration of process flow for generating 22nm STI array.

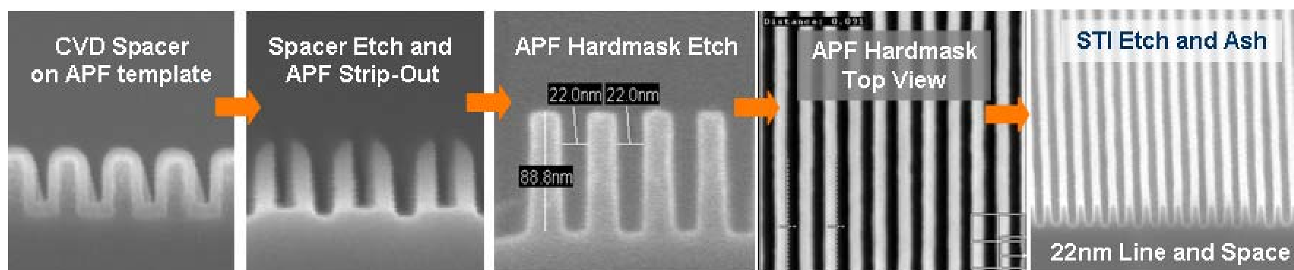
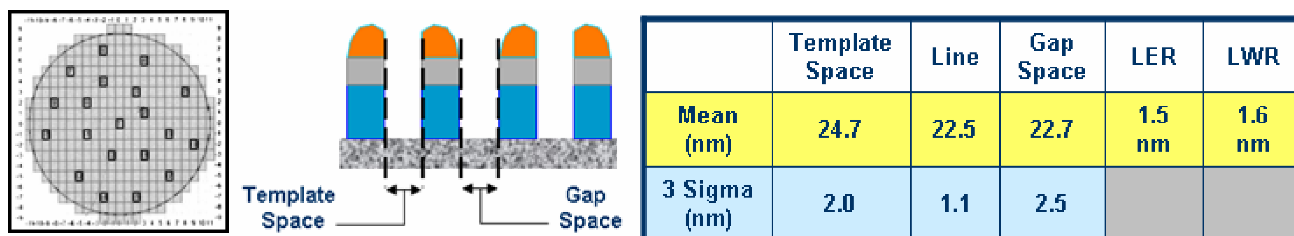


Figure 3: SEM image snapshots throughout process flow.



	Template Space	Line	Gap Space	LER	LWR
Mean (nm)	24.7	22.5	22.7	1.5 nm	1.6 nm
3 Sigma (nm)	2.0	1.1	2.5		

Figure 4: Typical CD performance from the dual APF SADP process flow.

2.2 Cutting the 22nm array into GDR structures

To manipulate the 22nm array into various examples of GDR structures, we overlaid cut masks above the patterned STI. In this case, we did not have purpose-built masks for making specifically engineered structures; therefore, we took some conventional 45nm node via link structures and forced them to overlay using an ASML 1400e scanner. Figure 5 shows examples printed without BARC to illustrate how the structures overlay and examples with BARC which were used for the actual cutting process. Additionally, Figure 6 shows the superposition of the masks over the STI array before and after BARC etch.

Finally, a silicon etch was performed to cut the once continuous array of STI into a 22nm active areas comprised of both long lines and small islands mixed densely together. The completed examples of 22nm densely packed GDR structures are shown in Figure 7. Therefore, we successfully achieved the objective, which was to combine the newest SADP patterning strategies being implemented at aggressive geometries for NAND FLASH devices with the arising concept of using cross-cut double patterned lines for creating GDR structures that could pave the way for new designs of logic and other devices. And is this case, we demonstrated the feasibility of creating 22nm half-pitch circuits using conventional wafer fab equipment.

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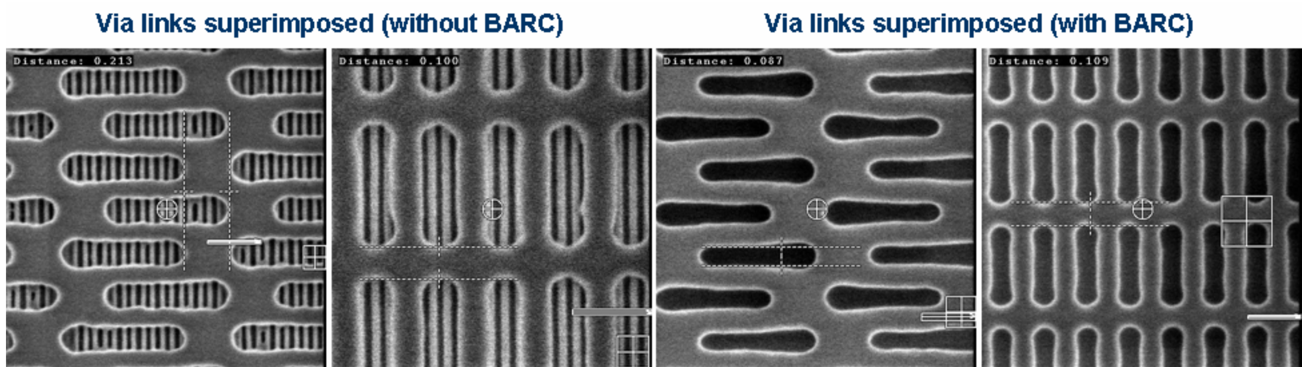

Figure 5: Cut masks patterned over the 22nm STI array. Printed without BARC (left) for example only of superposition and printed with BARC (right) which as used for manufacturing cuts.

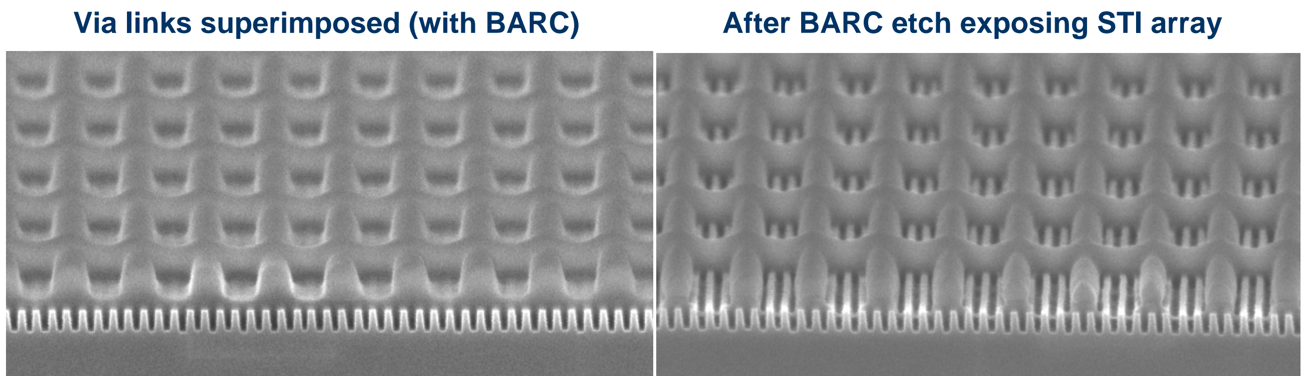

Figure 6: Tilt view of cut mask superimposed over the STI array. As printed (left) and after BARC etch (right)

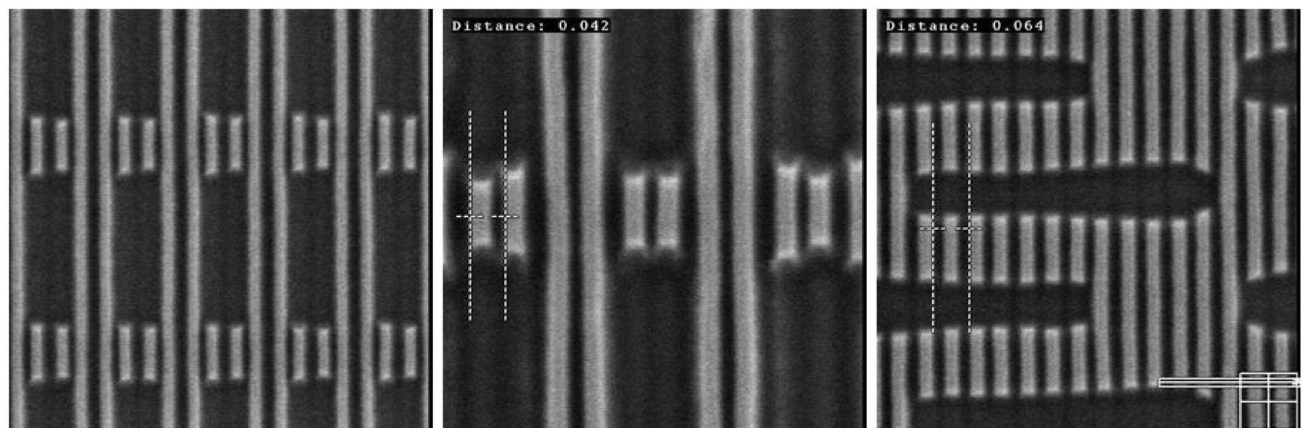

Figure 7. Examples of 22nm half-pitch GDR structures patterned into silicon. The Structures are manufactured using an SADP spacer hardmask scheme in conjunction with a cut mask.

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3. CIRCUIT FUNCTIONS IMPLEMENTED USING THE TELA CANVAS™

The pitch-halving technique described in section 2.1 works very well for grating patterns like NAND FLASH memory array active "sticks," bitlines, and wordlines. The challenge for logic is to use a process as described in section 2.2 to split the array lines into segments useful for circuit functions. A design style which uses regular structures is more suitable for low k_1 lithography and pitch halving [10].

The section 2 description of the pitch-halving applies to active/STI, as illustrated in the figures. It also can apply to the gate pattern, as mentioned in the references. The following sections give examples of the SADP applied to the gate level of CMOS circuits.

3.1 SRAM application

SRAM bit cells have used two patterning steps since at least the 45nm technology node [8]. This approach has been considered for over 12 years and has been well documented (see for example [7,9]). The gates are first patterned as long, parallel lines extending across the memory array. A second pattern using slots perpendicular to the gate lines is then used to cut the gates into segments. These segments form the 6 transistors of a conventional SRAM cell. Figure 8 shows an example of the active and gate layout, including where the cuts are made.

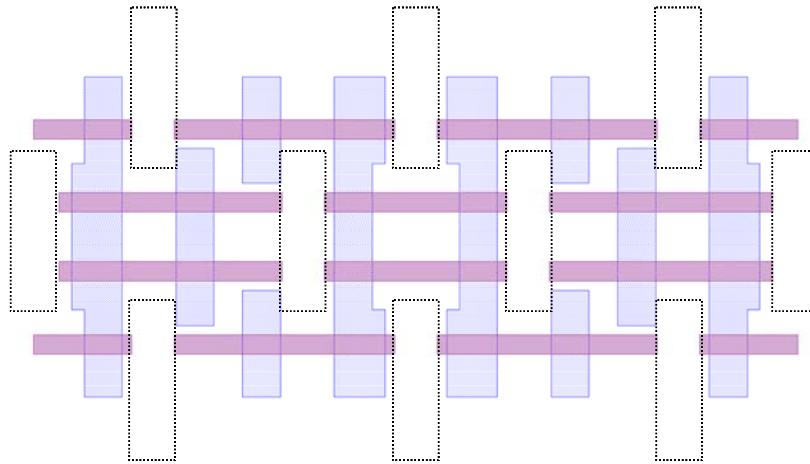

Figure 8. SRAM cell layout with vertical active regions, horizontal gate stripes, and gate-cuts (dashed boxes).

Because of the regular, repeating pattern in the SRAM array, the gate lines can be cut in pairs by the cut mask. The mask is needed because end-rounding and end-pullback would require more overlap of the active regions by the gates to ensure that the full transistor length is maintained across each transistor channel. Extra gate overlap would increase the width of each bit cell, a factor which is amplified by the number of columns in a typical array.

The impact of end-rounding and end-pullback is going to get worse at 32nm and 22nm as the lithography k_1 gets lower. Since the cut mask will be needed for the SRAM bit cell, it should be usable in other parts of a chip as long as the design style has regularity similar to an SRAM array.

3.2 Logic GDR layouts which can use SADP and gate cutting

Conventional random logic has a layout with many 2D patterns and many combinations of widths and spaces. To take advantage of the finer pitch provided by SADP, a highly regular design style like the Tela Canvas™ is needed. The following examples show how different circuit functions can be realized using SADP and a cut mask.

One of the building blocks of digital logic is the inverter. The output Q- is the logical inverse of the input Q. Figure 9a shows the schematic of a CMOS inverter. The NMOS and PMOS transistors have common gates and drains. The sources are tied to supply rails. A partial layout of the inverter is shown in Figure 9b. Horizontal metal tracks are shown for reference to indicate n+ and p+ active region sizes and their relationship. Vertical gates are also shown as they would appear in a final circuit. Figure 9c shows the initial layout of the gates as well as the cut mask slots needed to separate gate lines at the cell top and bottom edges. For this kind of circuit, no cuts are needed in the interior of the cell.

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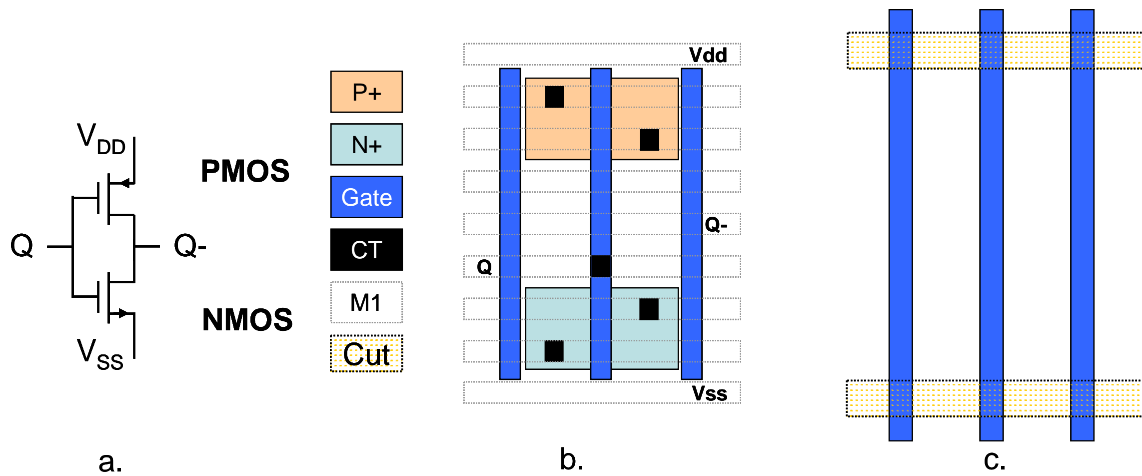

Figure 9. CMOS inverter: a. schematic, b. layout, and c. illustration of the gate and cut masks.

Another important building block for digital logic is the transmission gate shown in Figure 10. The circuit functions to pass a signal from the input to the output through the parallel NMOS and PMOS transistors Figure 10a shows the schematic of the CMOS transmission gate. The NMOS and PMOS transistors have common sources and drains. The gates are tied to control signals which are the logical inverse of each other. A partial layout of the transmission gate is shown in Figure 10b. As before, horizontal metal tracks are shown for reference to indicate n+ and p+ active region sizes and their relationship. Vertical gates are also shown as they would appear in a final circuit. Figure 10c shows the initial layout of the gates as well as the cut mask slots needed to separate gate lines. Notice that for this logic function, cuts are needed at the top, bottom, and interior of the cell. Although Figure 10 shows an interior cut used only for the actual transistor gate, the cut could extend across all three gate lines.

These cells can be combined into more complex cells, also utilizing the SADP process described in section 2. Figure 11 is an illustration of how the vertical line pattern from Figure 7 could be used to form the gates of adjacent inverter and transmission gate cells. The N+ and P+ active regions could be formed using a line plus cut approach, with SADP used depending on the widths of the transistors (the height of the active regions). The width of the cut line could be reduced by a resist-shrinkage step if needed, allowing more vertical room for wider transistors.

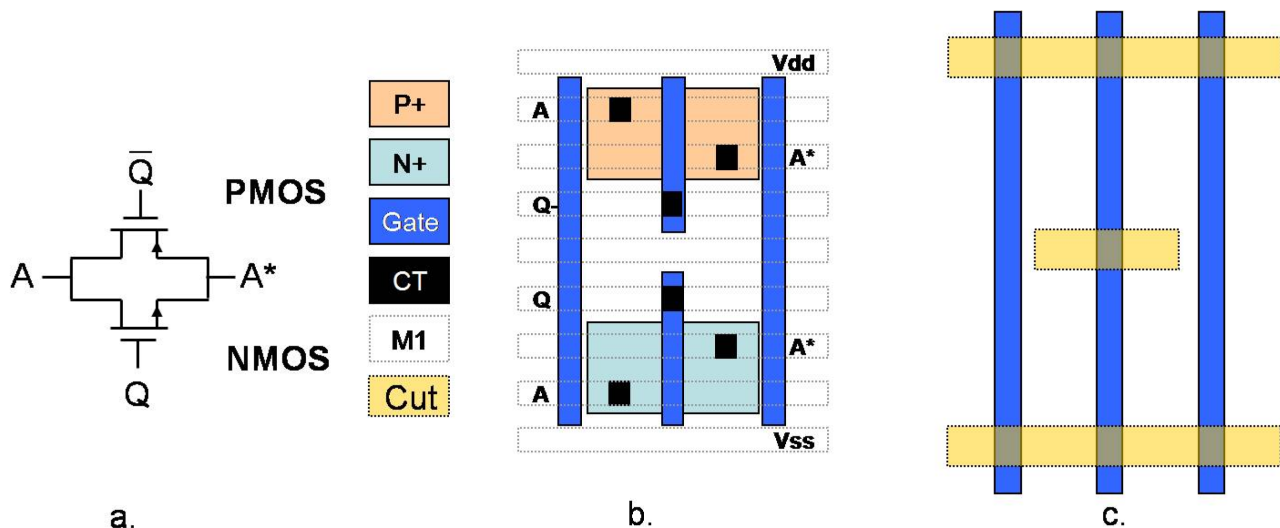

Figure 10. CMOS transmission gate: a. schematic, b. layout, and c. illustration of the gate and cut masks.

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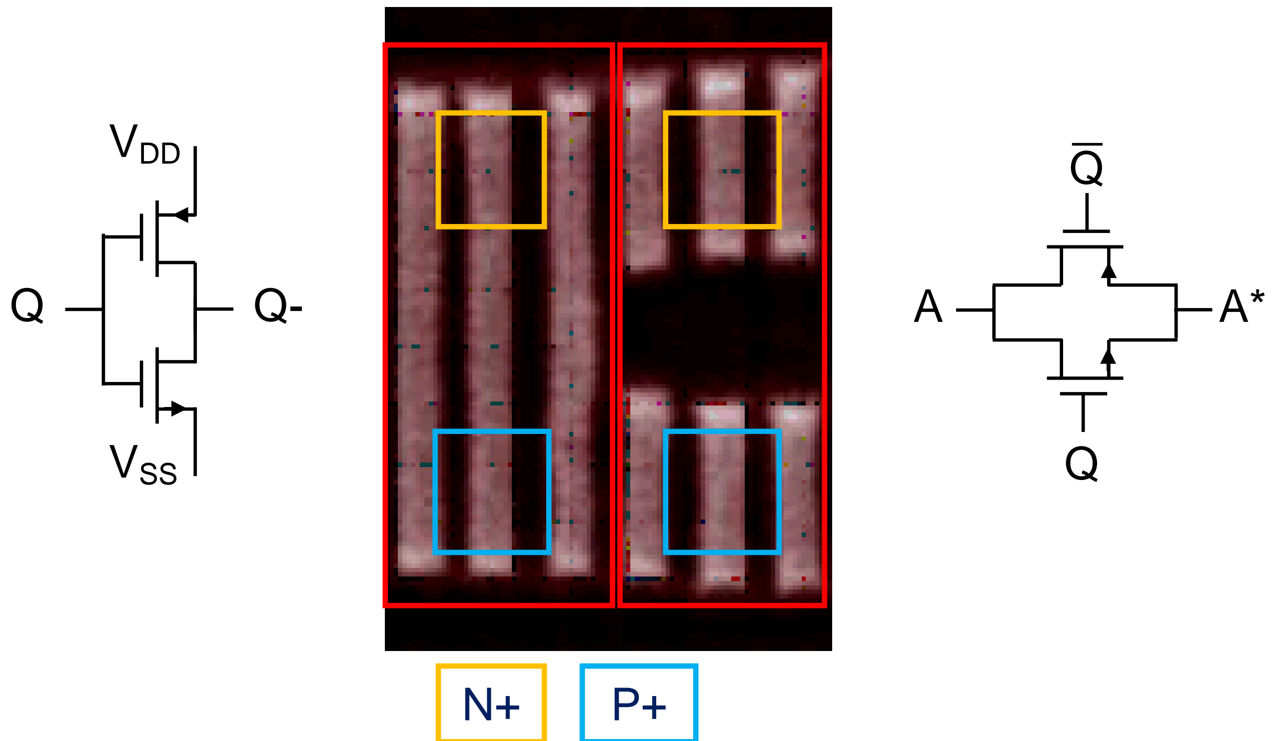

Figure 11. Illustration of how a combination of inverter and CMOS transmission gate could be built using the line pattern from Figure 7 for the gates.

4. CONCLUSIONS

The combination of an APF-based pitch halving process sequence and Tela Canvas™ design style has been used to demonstrate 22nm half-pitch GDR structures suitable for the 16nm logic technology node and beyond. These are expected to provide a cost-effective alternative to double (triple) exposure processes and EUV lithography.

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