22nm Logic Lithography in the Presence of Local Interconnect

Michael C. Smayling*[a], Robert J. Socha[b], Mircea V. Dusa[b]
[a]Tela Innovations, Inc., 655 Technology Pkwy.-, Suite 150, Campbell, CA, USA 95008
[b]ASML, 4211 Burton Dr., Santa Clara, CA, USA 95054

ABSTRACT

The 22nm logic node is being approached from at least two different scaling paths. One approach "B" will use Gate and 1x Metal pitches of approximately 80nm, which, combined with the appropriate design style, may allow single exposure to be used. The other combination under consideration "A" will have a Gate pitch of ~90nm and a 1x Metal pitch of 70nm. Even with immersion scanners, the Rayleigh k_1 factor is below 0.32 for 90nm pitch and below the single exposure resolution limits when the pitch is below 80nm.

Although highly regular gridded patterns help [1,2,3], one of the critical issues for 22nm patterning is Contact and Via patterning. The lines / cuts approach works well for the poly and interconnect layers, but the "hole" layers have less benefit from gridded designs and remain a big challenge for patterning.

One approach to reduce the lithography optimization problem is to reconsider the interconnection stack. The Contact layer is complex because it is connecting two layers on the bottom – Active and Gate – to one layer on the top. Other layers such as Via-1 only have one layer on the bottom.

A potential solution is a Local Interconnect layer. This layer could be formed as part of the salicide process module, where a patterned etch would replace the blanket strip of un-reacted metal of the silicide layer. Local interconnect lines would run parallel to the Gate electrodes, eliminating "wrong-way" lines in the Active layer. Depending on the final pitch chosen, Local Interconnect could be single or double patterned, or could be done with a self-aligned process plus a cut mask.

Example layouts of standard cells have shown a significant benefit with local interconnects. For example, the Contact count is reduced by ~25%, and in many cases Via-1 and Metal-2 usage was eliminated.

The simplified Active pattern, along with reduced contact count and density, permit a different lithography optimization for the cells designed with Local Interconnect. Metal-1 complexity was also reduced. Details of lithography optimization results for critical layers, Active, Gate, Local Interconnect, Contact, and Metal-1 will be presented.

Keywords: Low k_1, gridded design rules, restricted design rules, self-aligned structures, source-mask-optimization

1. INTRODUCTION

No improvement in fundamental optical resolution has been available since 1.35 NA immersion scanners [4] were introduced in 2007. With λ/NA = 143nm, the Rayleigh equation CD = k_1 λ/NA implies that further improvements in resolution depend on k_1.

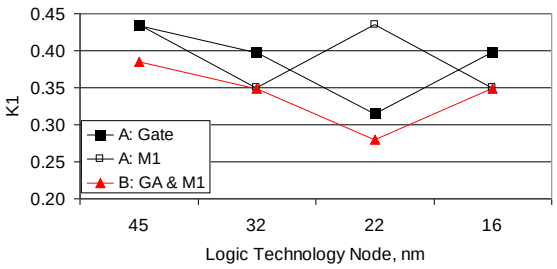

Fig. 1. k_1 trend for sub-65nm logic technology nodes

k_1 has been decreasing for recent logic technology node as shown in Figure 1. To maintain pattern fidelity at k_1 values below ~0.6, resolution enhancement techniques (RET) such as optical proximity correction (OPC), off-axis illumination (OAI), and phase shift masks (PSM) have been introduced. Pitch division is needed for the "A" scaling path Metal-1 at 22nm, and for both Gate and Metal-1 for both "A" and "B" scaling paths at 16nm.

*mike@tela-inc.com; phone +1 408 558-6321; fax +1 408 559-4600

As k_1 decreases, "practical limits" are imposed by the design style.[5] 2D layouts with bent polygons are limited to ~0.35. A 1D layout style with parallel straight lines looking much like a grating pattern, and has a limit of ~0.28. Extensive efforts are being made to define "restricted design rules" which allow bends but with constraints on widths or spaces.[6] A 1D layout style with further requirements for keeping lines on a regular grid permits using a simplified set of design rules described as "gridded design rules" (GDR).[7,8] Source-mask-optimization is becoming increasingly important, and benefits from the gridded design style. [9,10,11]

2. LAYOUT WITH LOCAL INTERCONNECT

2.1 Layout considerations at 22nm

At the extremely low k_1 values expected at 22nm, patterns with more grating-like appearance have better process windows. This means that bends, jogs, and "wrong-way" features should be avoided or minimized. In particular, the Active layer in previous generations has had connections to the power rails which make the layer look very 2D. Making the Active layer with only rectangles is one possibility, but this increases area since transistors of different widths need to be separated even if they share a common node.

2.2 Benefits of Local Interconnect

Examples of a cell layout without and with Local Interconnect are shown in Figures 2a and 2b, respectively. The Active layer, shown in light blue, is clearly more regular in the LI case. The power wires have been eliminated by LI straps in all cases. The number of contacts is reduced by about 25%. Not shown in these figures are the metal and via layers. For the LI layout, metal-2 usage was completely eliminated; this reduced the number of contacts, metal-1 lines, and eliminated vias.

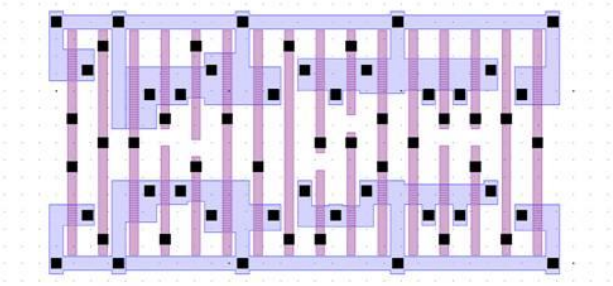

Fig.2a. Conventional Layout

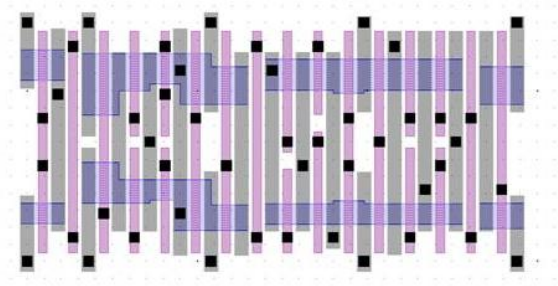

Fig.2b. Layout with Local Interconnect.

A similar exercise performed on an SRAM cell allowed a >20% reduction in area. Those results are reported elsewhere in this conference.[7641-5]

Depending on the method of implementing Local Interconnect, the ability to avoid Active contacts adjacent to transistor channel regions allows the full impact of mobility increase due to strain layers to be realized. In the layout without Local Interconnect, Active contacts are predominately adjacent to transistor channels, causing a reduction in the strain layer effectiveness in those transistors. The layout with Local Interconnect shows how the number of such Active contacts can be greatly reduced, improving the speed performance and modeling predictability of cells designed with Local Interconnect.

An additional benefit of Local Interconnect was found during the simulations for this project. The use of Local Interconnect as shown in Figure 2b allowed additional choices for the placement of contacts and the usage of metal-1 lines. Local Interconnect permitted spreading out the patterning difficulty normally associated with contacts and metal-1 across three patterning layers instead of two.

3. SIMULATIONS AND OPTIMIZATION

3.1 Software

The ASML Brion Tachyon SMO was used to optimize the FlexRay source and mask. Tachyon SMO minimizes the maximum edge-placement-error (EPE) at user defined process window (PW) conditions. The EPE is minimized by simultaneous optimization of the mask and illumination. The following six process window conditions were used: (±40nm defocus, best dose, no mask error), (best focus, ±3% delta dose, no mask error), and (best focus, best dose, ±0.5nm mask error). In the optimizations, the mask error contributed the most to EPE; consequently, MEEF minimization dominated the optimization. The MEEF minimization was especially important for dark field contact holes.

The minimization of the EPE is visualized by examining the process variation band (PV band) at the six PW conditions. The PV band can then be examined through a lithography manufacturing check (LMC) via Tachyon LMC. Tachyon LMC reports the defects, locations that have large PW variation. In addition to LMC check, Tachyon SMO calculates the process window at user selected cut lines, and these process window results are shown in the following sections.

3.2 Optimization flow

Once an initial set of basic design rules (width, space, end-gap for lines) were established for each critical layer, layouts were done for six representative standard cells. As shown in Figure 3, these cells were placed in a small block with different neighbors, and then the metal-1 was filled to give uniform end-gaps. The fill was kept on a separate layer to give flexibility in the subsequent lithography optimization. The block dimensions were approximately 16μm wide by 6.5μm high.

Fig. 3. Metal-1 layer of block with six different logic functions.

Simulations were run on the layouts to assess the process window under optimized illumination conditions. Since the pitches were fixed by the technology node targets, the primary design variable adjusted in each iteration was the end-gap. For example, in metal-1, end-gaps of 40nm, 50nm, and 54nm were studied.

Because of the gridded layout, other pitch combinations were studied. These included the Gate pitch / Metal-1 pitch of 80nm / 80nm, 78nm / 82nm, 76nm / 84nm, and 74nm / 86nm. Each combination of pitches was designed with- and without Local Interconnect. These pitch combinations were helpful to assess contact patterning options.

3.3 Contact results

For the contact hole, Tachyon SMO was used to minimize the EPE at the six PW conditions. The first attempt was to print the contact holes with single exposure (SE) and with a dark field mask. The PW was insufficient at this aggressive

half pitch of 40nm (k1=0.28). Therefore, a double patterning technique (DPT) was investigated by splitting the contact holes into two exposures using a litho-etch-litho-etch technique (LELE). Using Tachyon DPT, the contact hole pattern was split into two exposures. For these two exposures, a dark field mask and bright field mask were tested to determine which had the largest PW. Both dark field and bright field use a positive photoresist. The dark field mask uses an alkaline developer, while the bright field mask uses a solvent developer [12]. The simulated PW results of the bright field and dark field mask for the DPT are shown in Figure 4. The dark field PW has maximum exposure latitude (EL) of 4% which is insufficient. The bright field mask, however, has a large process with 90nm DOF at 5% exposure latitude. The large maximum EL of the bright field mask also lead to a lower maximum MEEF of 4.3, while dark field mask lead to a higher maximum MEEF of 9.1.

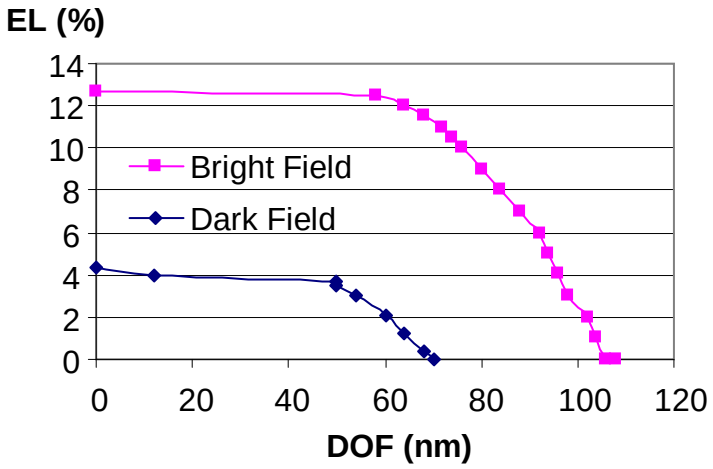

Figure 4. Simulated Contact Hole Process Window created through a dark field mask or through a bright field mask.

The mask and illumination is shown in Figure 5 for first exposure bright field contact hole. Using the contact holes on the first exposure target design, SMO simultaneously optimized the mask and illumination. The SRAFs were constrained to be rectangular rather than freeform polygonal SRAFs. The illumination pupil also uses all the constraints of the FlexRay illumination; thus, it guaranteed to implementable on the ASML scanner. The PV band at the six process window conditions is also shown. The PV band is very tight which leads to the large PW and low MEEF.

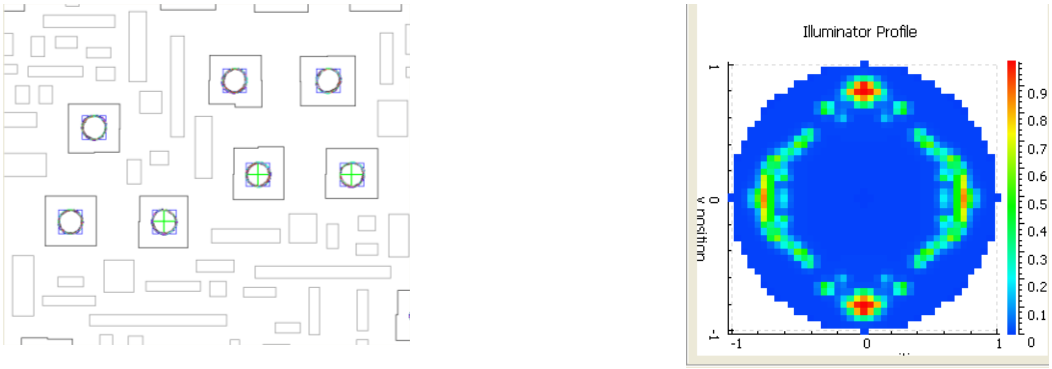

Figure 5. The contact hole bright field mask, and the FlexRay illumination pupil for the 80/80 design. The mask is for the first exposure. The target CD is the blue polygon, and the OPC and SRAFs are in black and gray, respectively.

Since the contact hole required DPT, the trade off between the design and PW window was examined through a symmetric shrink (horizontal and vertical minimum pitch of 80nm each, k1=0.28) and through an asymmetric shrink (horizontal minimum pitch of 74nm, k1=0.26, and vertical minimum pitch of 86nm, k1=0.30). In Figure 6, the 74/86 design was able increase the maximum DOF to 118nm compared to 108nm for 80/80 design. Since this increase is small and the PW of 80/80nm design was sufficient, the metal 1 and local interconnect (LI) results in the next two sections use the 80/80 design.

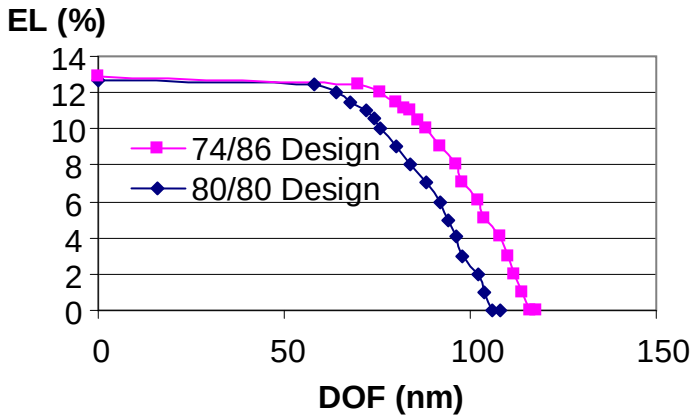

Figure 6. Simulated Contact Hole Process Window with different horizontal and vertical minimum pitches. The 80/80 Design has a minimum horizontal pitch of 80nm and a minimum vertical pitch of 80nm. The 74/86 Design has a minimum horizontal pitch of 74nm and a minimum vertical pitch of 86nm. The 74/86 Design has slightly larger DOF, but the DOF of the 80/80 Design is sufficient.

3.4 Metal-1 results

Tachyon SMO was used to optimize the binary dark field mask and illumination for the metal 1 layer, and the PW was calculated. In Figure 7, the PW was simulated for two different metal 1 designs. The minimum gap between to trenches was varied from 50nm (aggressive) to 54nm (less aggressive). The PW for the 50nm and 54nm gap are almost identical. However, the maximum MEEF of the 54nm gap is 7.7 and the maximum MEEF of the 50nm gap is 9.1. Although the MEEF is higher for the 50nm gap, the contact and via coverage of the metal 1 is critical, and a high MEEF may be tolerable if the coverage is sufficient. The trade-off between metal-1 gap and contact overlap is straightforward with the gridded layout. The metal-1 layer has the additional optimization factor of using the fill pattern. The optimizer has the choice of removing a fill geometry, treating the fill geometry as a sub-resolution feature, or changing the linewidth target for lines adjacent to fill lines.

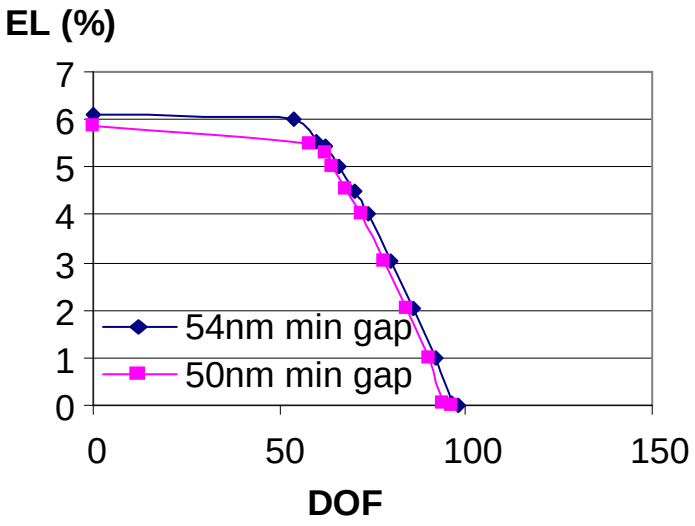

Figure 7. Simulated Metal 1 Process Window with different minimum gap separation of 50nm and 54nm. The PW are same for the 50nm and 54nm gap. The MEEF of the 54nm, however, does decrease. The MEEF of the 54nm gap is 7.7 while the MEEF of the 50nm gap is 9.1.

3.5 Local Interconnect results

Tachyon SMO optimized the binary dark field mask and illumination for the local interconnect with results shown in Figure 8. The local interconnect is unidirectional with lines orientated in the vertical direction. Because of the unidirectionality of the lines, the illumination has a strong dipole element. The end of the trenches are primarily corrected through OPC (bias and SRAF); however, the illumination does have some energy at the top and bottom of the pupil. The EPE minimization was dominated by the mask error. This is seen in figure 8 where the smallest contour is for a mask error of -0.5nm and the largest contour is for a mask error of +0.5nm. The contours of defocus and dose errors are inside the contours of the mask error. Thus the optimization is dominated by minimizing the MEEF. Like the case of metal 1, minimization of the mask error may not be the most important constraint if the contact and via coverage is sufficient.

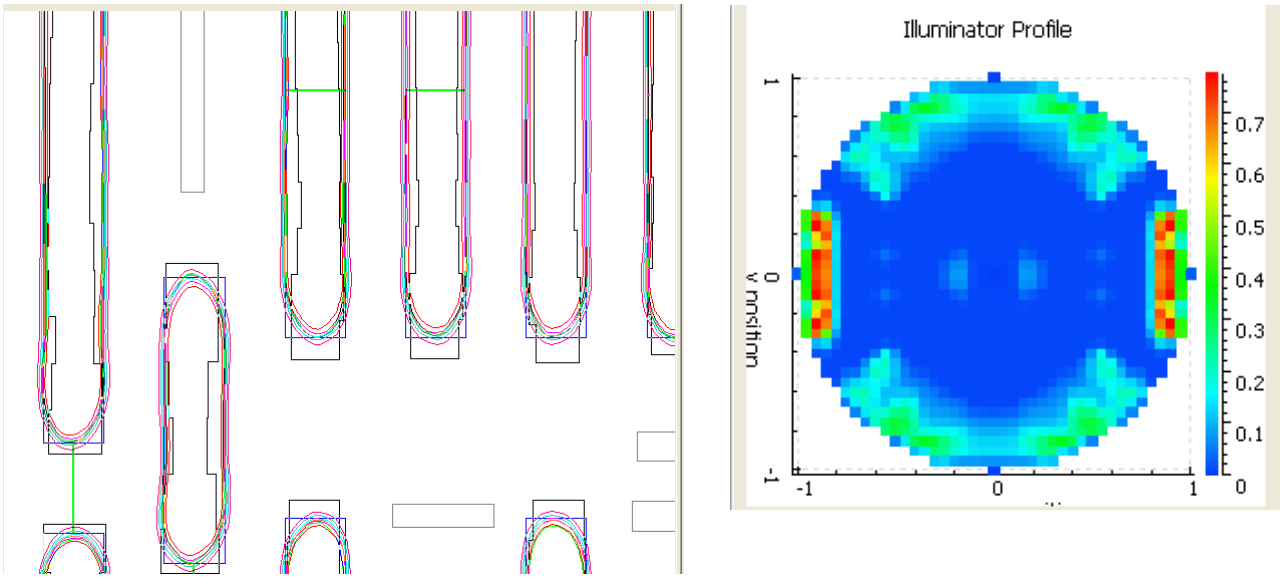

Figure 8. The local interconnect dark field binary mask, and the FlexRay illumination pupil. The target pattern is the blue polygon, and the OPC and SRAFs are in black and gray, respectively. The PV band of the six PW conditions is also shown. The PV band is dominated by the mask error.

In Figure 8, the PV band is largest at the end of the trenches while the long vertical direction has little process variation. This large process variation band at the end of the trenches is seen in the PW shown in Figure 9. In Figure 9, the PW is constrained by the end of the trenches. The PW window has 80nm DOF at 5% exposure latitude. Similar for metal 1, if the coverage of the contacts and vias are sufficient for the PW conditions, the PW analysis is less important, and the traditional PW metric for lithography needs to be examined in the context of the design.

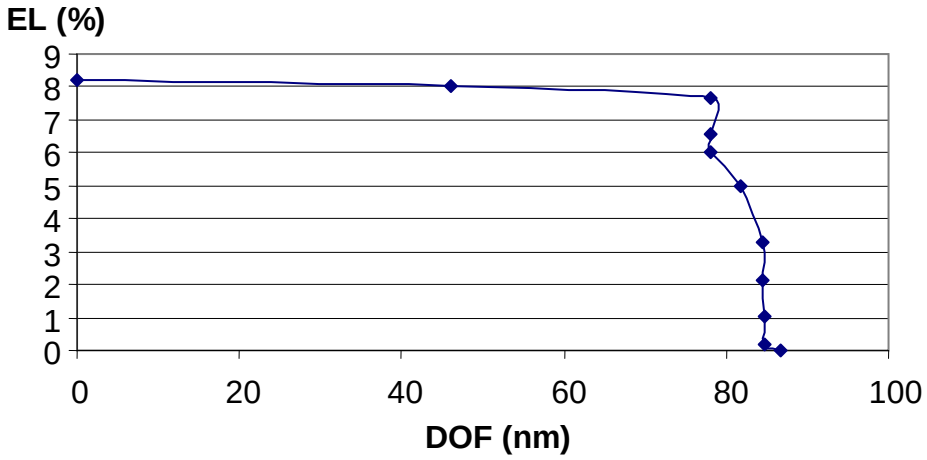

Figure 9. Simulated Local Interconnect (LI) Process Window. The PW is dominated by maximizing the PW of the end of the trenches.

4. CONCLUSIONS

Single exposure patterning at the 22nm node should be possible using scaling path "B" in which the gate pitch and metal-1 pitch are both 80nm. Within the pitch constraints, the line end-gap was adjusted to give a reasonable process window.

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