Inter-layer Self-Aligning Process for 22nm Logic

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ABSTRACT

Line/space dimensions for 22nm logic are expected to be ~35nm at ~70nm pitch for metal 1. However, the contacted gate pitch will be ~90nm because of contact-to-gate spacing limited by alignment. A process for self-aligning contact to gates and diffusions could reduce the gate pitch and hence directly reduce logic and memory cells sizes.

Self-aligned processes have been in use for many years. DRAMs have had bit-line and storage-node contacts defined in the critical direction by the row-lines. More recently, intra-layer self-alignment has been introduced with spacer double patterning, in which pitch division is accomplished using sidewall spacers defined by a removable core.[1] This approach has been extended with pitch division by 4 to the 7nm node.[2]

The introduction of logic design styles which use strictly one-directional lines for the critical levels gives the opportunity for extending self-alignment to inter-layer applications in logic and SRAMs. Although Gridded Design Rules have been demonstrated to give area-competitive layouts at existing 90, 65, and 45nm logic nodes while reducing CD variability[3], process extensions are required at advanced nodes like 22nm to take full advantage of the regular layouts.

An inter-layer self-aligning process has been demonstrated with both simulations and short-loop wafers. An extension of the critical illumination step for active and gate contacts will be described.

Keywords: Gridded design rules, restricted design rules, self-aligned structures

1. INTRODUCTION

The era of continual improvement in patterning equipment resolution has ended, with no improvement in optical performance since 1.35NA immersion scanners [4] were introduced in 2007. With λ/NA = 143nm, the Rayleigh equation CD = k_1 λ/NA implies that further improvements in resolution depend on k_1.

k_1 has been decreasing for recent logic technology node as shown in Figure 1. To maintain pattern fidelity at k_1 values below ~0.6, resolution enhancement techniques (RET) such as optical proximity correction (OPC), off-axis illumination (OAI), and phase shift masks (PSM) have been introduced. Note that the "22S" point is not realizable with k_1< 0.25.

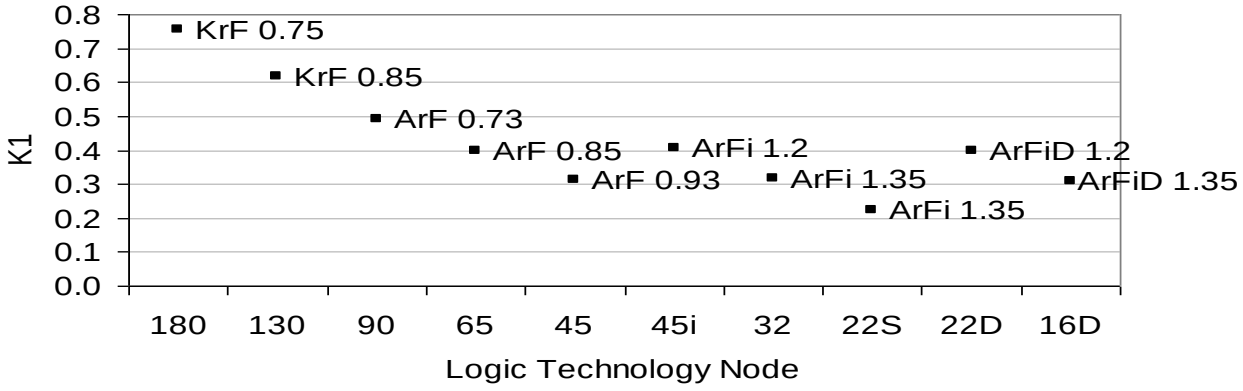

Fig. 1. k_1 trend for sub-200nm logic technology nodes.

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As k_1 decreases, "practical limits" are imposed by the design style.[5] 2D layouts with bent polygons are limited to ~0.35. A 1D layout style with parallel straight lines looking much like a grating pattern, and has a limit of ~0.28. Extensive efforts are being made to define "restricted design rules" which allow bends but with constraints on widths or spaces.[6] A 1D layout style with further requirements for keeping lines on a regular grid permits using a simplified set of design rules described as "gridded design rules" (GDR).[7,8]

2. SELF-ALIGNING PROCESS

2.1 Importance of contacted-gate pitch

Even with gridded design rules, logic elements like standard cells are limited by the grid pitch in the X and Y directions. As shown in Figure 2, with gate electrodes in a vertical direction, and metal-1 wires in the horizontal direction, the logic cell area is set by the number of lines in each direction multiplied by the pitch for those lines. The metal-1 pitch is set purely by lithography resolution, and can be extended for many nodes by using pitch division.[2]

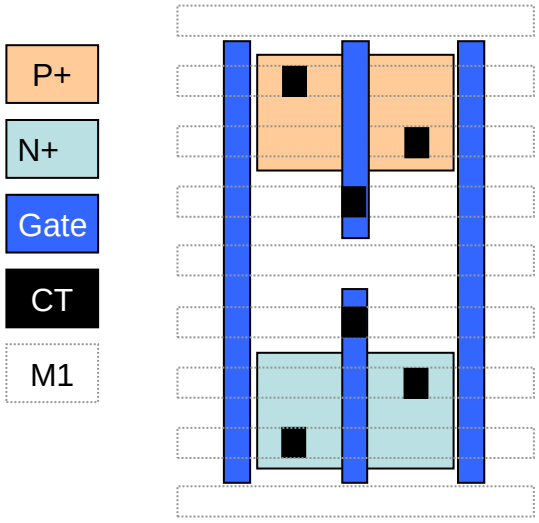

Figure 2. Logic inverter layout showing transistor layers.

However, the gate pitch is limited by both intra-layer resolution and inter-layer alignment between the gates and adjacent active contacts as shown in Figure 3. Anything done to reduce the contact-to-gate-space will directly improve cell area.

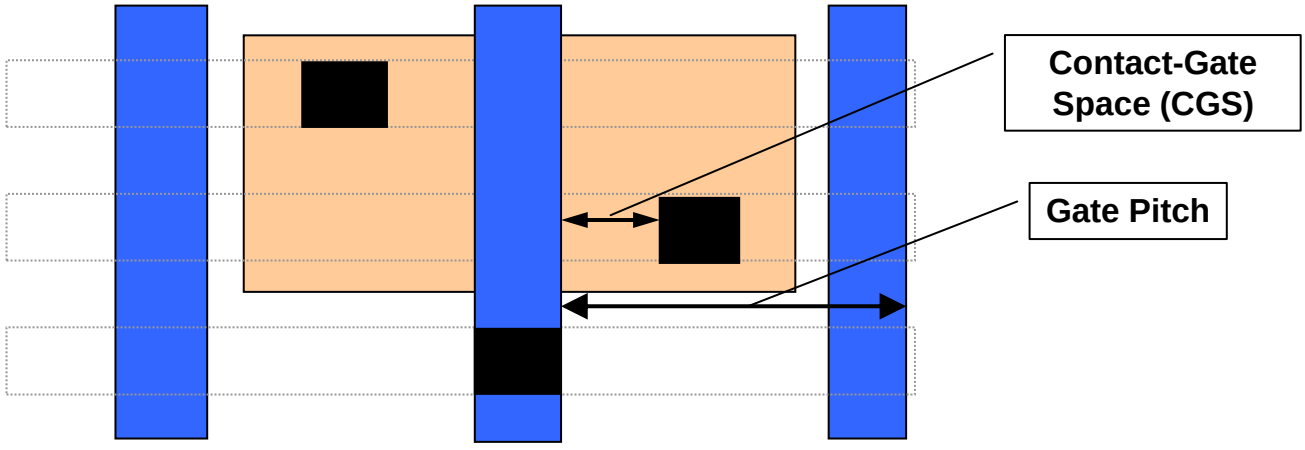

Figure 3. Detail of contacted-gate pitch.

Since both the active and gate contacts are on a grid set by the gates in the horizontal direction, this 1D gridded style has the potential to use the gate location to align contacts either to the gate or centered between the gates. This is not the case for conventional 2D random logic layout.

2.2 Structure to be evaluated

The self-aligning process involves multiple layers in the device structure, so additional structure information is needed to describe the steps. Figure 4 shows the cross-section of the structure to be tested in simulation and wafer form.

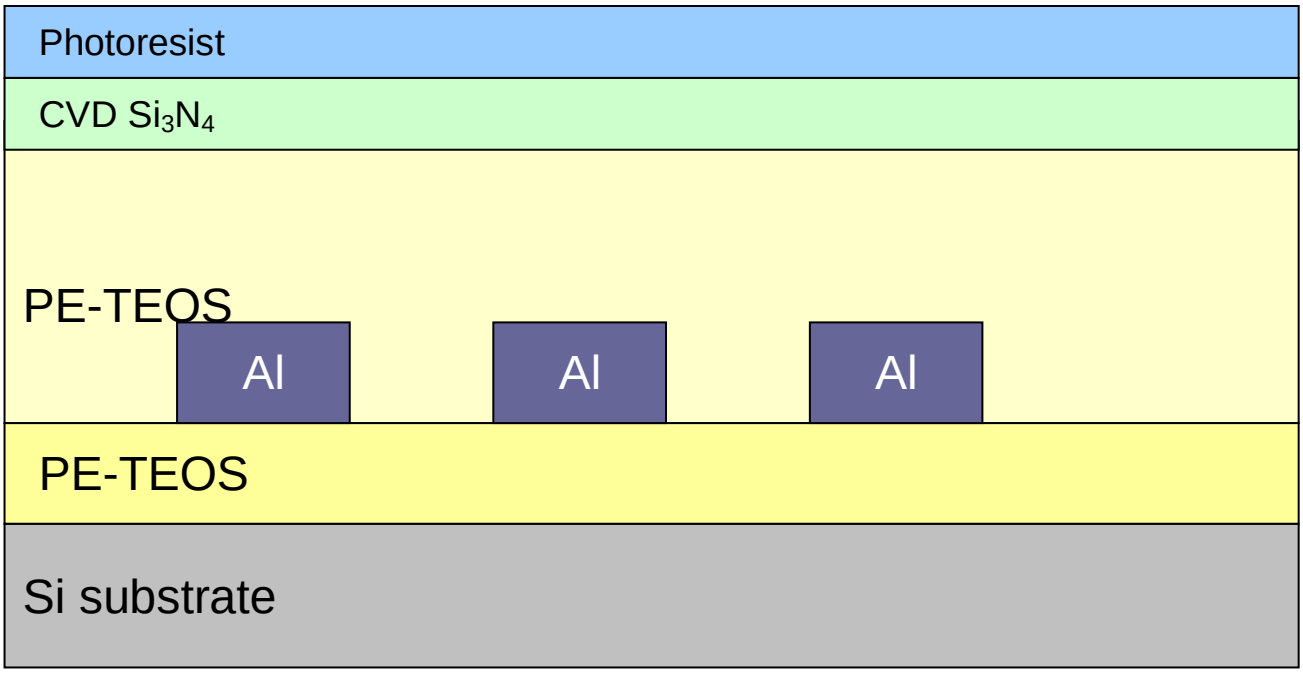

Figure 4. Cross-section of the structure under evaluation.

The structure in Figure 4 was fabricated at SVTC with standard process equipment and recipes. The gates were built with aluminum instead of silicided polysilicon for the first experiments to have better control of their optical properties. The upper plasma-enhanced TEOS layer was processed in several steps, with an intermediate CMP step to get a flat surface over the gates. The post-polish oxide thickness was measured, and then additional TEOS was deposited to reach the final target thickness over the gates. A silicon nitride layer was deposited to serve as a hardmask for subsequent self-alignment steps. A thin layer of photoresist was spun-on over the nitride to complete the structure preparation.

The critical step in the self-aligning sequence is the blanket illumination of the top layer of photoresist. Using the "wafer as a mask" allows a blanket illumination to be used. The exposure dose is an important factor; the dose is chosen such that regions of the resist which receive both incoming light as well as light reflected from the gates are above the develop threshold, while regions with only the incoming light are below the threshold. The resist can be positive or negative, and the develop process can be positive or negative, so either lines or trenches can be formed above the gates.

The experimental processing was completed up to the blanket illumination step. Future experiments are anticipated to complete a series of blanket deposition and etching steps to allow forming contacts which are self-aligned in the horizontal direction to either the gates or centered between the gates.

3. SIMULATIONS AND WAFER RESULTS

3.1 Simulations

Although many photolithography simulation tools can produce aerial images from source and mask data, many have an implicit assumption that there is no light reflected from the substrate. This is often not a good assumption, and in the case of the self-aligning process, reflected light is of paramount importance.

The recently introduced PROLITH X3 is ideally suited for simulations in which wafer topography has an impact on the patterning results. It can read in a GDS file with the underlying pattern, and use this in the preparation of the simulation substrate.

For simplicity, a cross-section was constructed with a single line having spaces on each side. Figure 5 shows the structure and the expected intensity pattern during the blanket illumination.

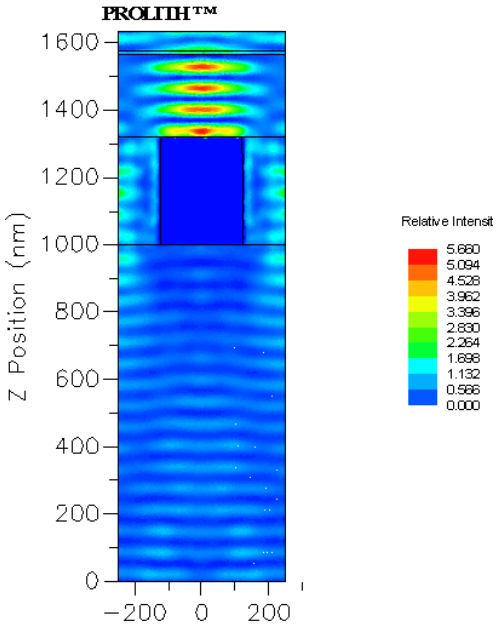

Figure 5. Prolith X3 simulation cross-section with a central line having gaps on each side.

As figure 5 shows, a pattern of standing waves is created above the central gate line. The gate is clearly reflecting light, while the gaps on either side are permitting light to pass deeper into the structure. There are several high intensity regions directly above the gate; control of the TEOS thickness is required to put a peak of intensity within the photoresist layer.

In addition to looking at the cross-sections to tune the stack thickness, aerial images were also created. For example, figure 6 shows a segment of a gate line and the resulting image based on the blanket illumination of the gate. The aerial image shows some bowing and widening compared to the original line width, and some line-end shortening. However, having this pattern in the resist above the hardmask can be useful for the self-aligning sequence since the aerial image is still congruent with the original pattern in the horizontal direction.

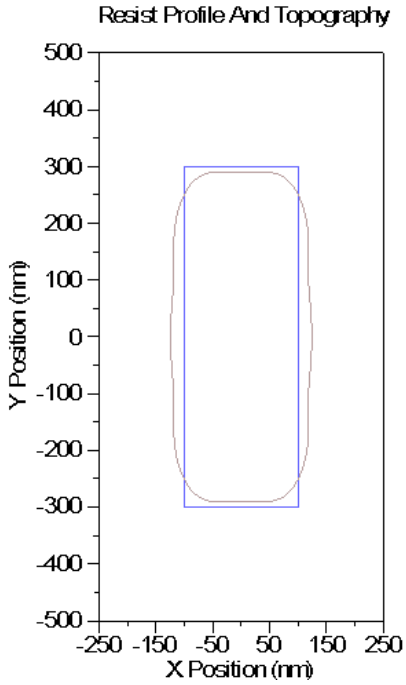

Figure 6. Aerial image (light brown) resulting from the original gate pattern (blue rectangle).

In addition to looking at just nominal conditions, simulations were done to look at the resist gap sensitivity to the underlying pattern line width as shown in Figure 7a. Further work is planned in the subwavelength regime. The gap width was also studied as a function of the film stack. Figure 7b shows the relationship with the nitride hardmask thickness; there is a 27.4nm change in linewidth for each 1nm change in nitride thickness, so process control is important.

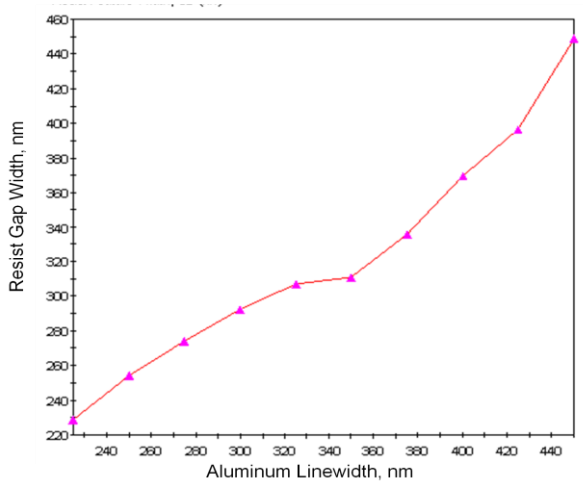

Figure 7a. Resist gap width versus mask width.

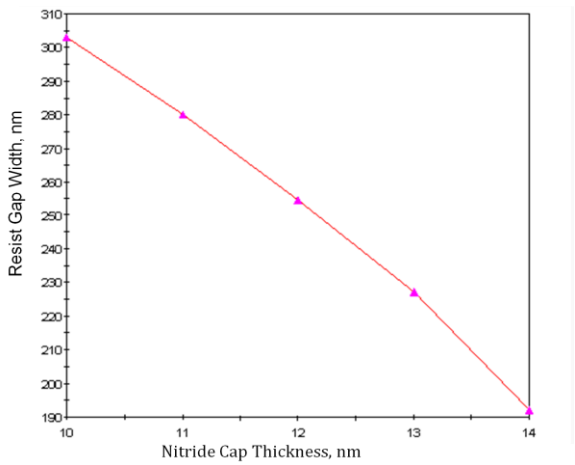

Figure 7b. Resist gap width versus nitride cap thickness.

The effect of a masked exposure was also studied. A slot wider than a contact is formed in the normal mask, then the wafer with an underlying pattern is exposed. Figure 8a-c shows the resulting final pattern in the top resist. Offset of the mask pattern was introduced to represent misalignment. The resulting pattern in the top resist had an offset reduced to a third of the original offset in the mask. The final CD was changed by less than 0.5% as a result of the offsets.

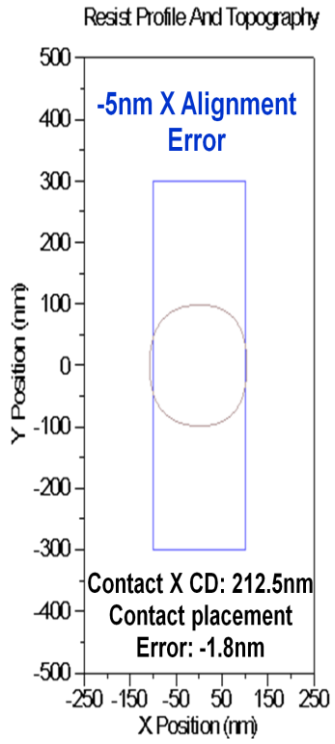

Fig. 8a. Slot exposure with -5nm alignment offset.

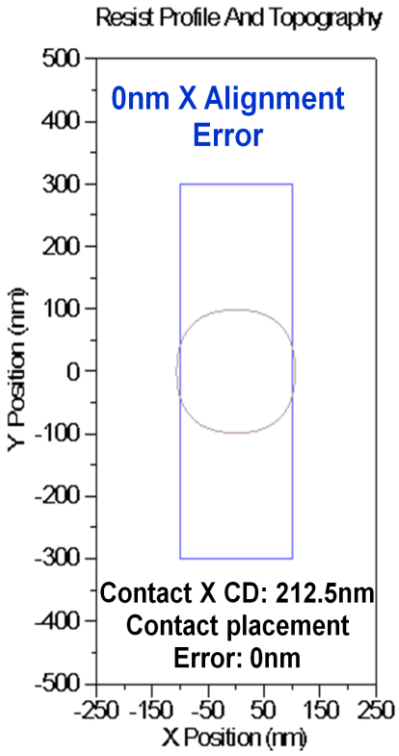

Fig. 8b. Slot exposure with 0nm alignment offset.

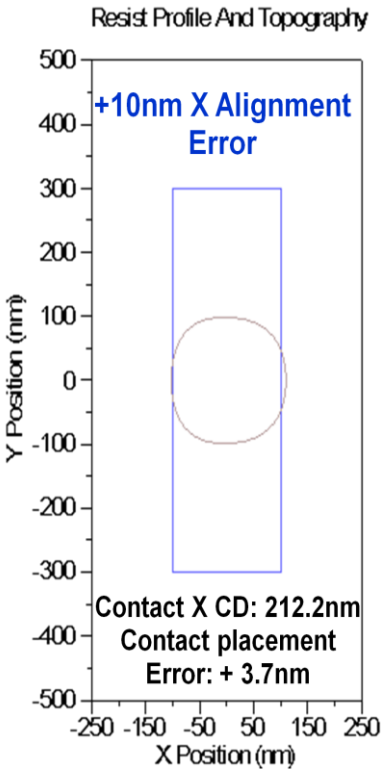

Fig. 8a. Slot exposure with +10nm alignment offset.

3.2 Wafer results

The critical step in the process sequence is the blanket illumination step. Test wafers were prepared with the film stack shown in figure 4. The oxide thickness above the aluminum lines was controlled by a measurement after CMP planarization, then an adjustment to the deposition time to achieve the desired final thickness. The thicknesses were initially simulated with Prolith and adjusted to get a reasonable intensity profile in the resist.

The photoresist type and deposition were adjusted to get the thin layer required. Shin-Etsu SXM-1754 was hand-dispensed with a thickness of 55.0nm with a sigma of 1%. Exposure was done with an ASML 1250XT (with no reticle pattern) to permit precise exposure control. An exposure matrix was run, with a dose of 3.2mJ/cm^2 giving the best results.

SEM photos are shown in Figures 9a and 9b. The top-down image in Figure 9a shows that the pattern of lines in the underlying aluminum gate layer was replicated into the resist lying on top of the hardmask. The line/space pattern as well as the line ends were resolved, as predicted b the simulations. The tilted SEM in Figure 9b shows that the resist was removed in the double-exposed regions as expected. However, work remains on the develop process to reduce edge roughness and eliminate any remaining resist in the exposed regions.

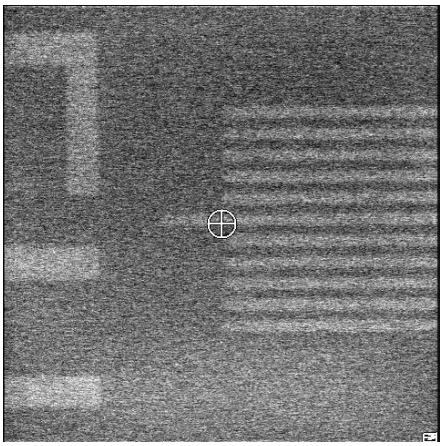

Figure 9a. Top-down SEM of the top resist pattern.

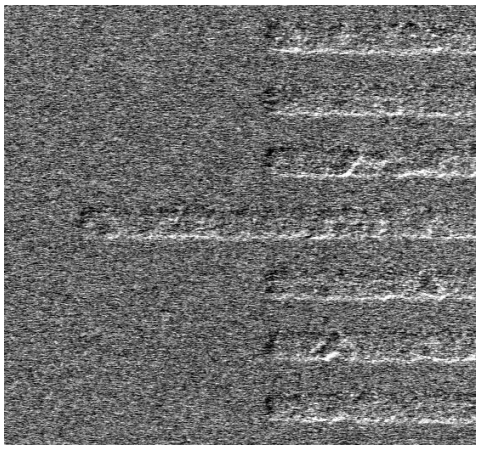

Figure 9b. Tilted SEM of the top resist pattern.

4. CONCLUSIONS

A self-aligning process, using the wafer-as-a-mask, has been simulated. This kind of process can be very useful to reduce logic cell size at the 22nm node where gate pitch is dependent on contact alignment. Wafer data have been presented down to 250nm linewidths. The new capabilities of PROLITH X3 have allowed the study of realistic logic cell layouts. The approach appears feasible for both gate and active contacts.

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