Supreme lithographic performance by simple mask layout based on lithography and layout co-optimization

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ABSTRACT

A method to resolve 20nm node of SRAM contact layer whose minimum pitch is 90nm with enough process latitude is shown. To achieve the target by single exposure under condition of Ar\textsubscript{F} and 1.35 of NA a way to optimize lithography parameters and layout parameters simultaneously is applied that is called co-optimization. At first the memory cell is optimized from several viewpoints of device and lithography, and then the entire memory cell block including the array circuit is optimized. It proves that combination of co-optimization and insertion of SRAF works very well considering the appropriate printed shape required by the device layout. The co-optimization is compared to such a conventional method as OPC. The performance is better than conventional OPC. Especially the MEEF is much better and the evaluation to find the mechanism is shown. It proves that complex patterns with many fragments make MEEF higher. The superior characteristics of co-optimization are analyzed by the result of Linear Programming that can find the strict solution. The pixel source shape has become almost same as one by co-optimization. The solution is achieved by binary mask with simple patterns and the simple source shape. It is crucial for COO.

Keywords: optimization, co-optimization, SMO, illumination, source, layout, OPC, Computational lithography

1. INTRODUCTION

EUV lithography has been long developed and the prototype tool and the relevant technologies have been ready for R\&D purpose, however it has not reached the mass production stage. So have other advanced lithography such as EB and NIL. The technologies might be applied to memory devices thanks to the limited patterns. In contrast logic devices have a variety of patterns and the lithography cannot be specific. So Ar\textsubscript{F} lithography is a sole candidate for advanced logic devices. Since lithography that can be applied to any patterns leads to less resolution, DP or ILT (Inverse Lithography Technology) are being considered for advanced logic devices. However DP needs twice the conventional process and in case of stitching process high accuracy of overlay is required. ILT needs the complicated mask pattern. Both have a problem of cost. Under this present situation we show a way to optimize device layout with the lithography condition. It can achieve supreme lithographic performance using simple mask layout and illumination source shape, which leads to better COO. We apply this technology to a contact layer of 20nm node SRAM under single exposure.

2. PRINCIPLE OF LITHOGRAPHY AND LAYOUT CO-OPTIMIZATION

2.1 Layout of contact layer

Figure1 shows layout of contact layer of 20nm node SRAM. All holes have the same size of 40nm. The layout has a basic block that consists of 16 holes. The size is 360nm x 960nm. The boundary is shown by rectangles in the figure. The entire layout is created by placing it periodically in x and y directions. The minimum pitch is 90nm in x direction, while the pitch in diagonal direction is 106nm. Since under Ar\textsubscript{F} lithography with NA 1.35 the k\textsubscript{1} is 0.31 for dense holes, double patterning process with pixel illumination source or application of complicated pixel mask pattern with pixel illumination source have been proposed to achieve the target [1], [2].
2.2 Principle of co-optimization

Each hole in the basic block is classified to groups with same circumstance of position according to the symmetry. In figure 2 the holes with the same circumstance are painted the same color. The number is index of each group. Shown in figure 3 individual hole has layout parameters of the length of sides (x, y) and the position deviation from the original design (dx, dy). The position parameters are used to compensate image shift of the holes. All holes in the entire layout can be expressed by these layout parameters using x/y-pitch of the block. Since there are 12 independent holes, this layout has 24 size parameters and 24 position parameters, totally 48 layout parameters.

The illumination source has parameters of outer and inner radius, intensity of x-pole/y-pole, and opening angle of x-pole/y-pole, in total 6 source parameters, shown in figure 4.

Then the layout parameters and the source parameters are combined together to create a composite parameter space. In this optimization space a lithography target is optimized by a heuristic method without discrimination of layout and source parameters. The key of this method is that the layout parameters and the source parameters are optimized simultaneously, while the conventional method optimizes them iteratively. We call this method co-optimization. The conventional iterative SMO has some disadvantages of more optimization steps and more probability trapped at local minima and the single SO or MO tends to find complicated solutions.

Since all layout parameters are optimized simultaneously, mutual interference of each hole is considered, which is hard for OPC that handles local edge placement under single simulation. Source has OPE (Optical Proximity Effect) whose concept leads to edge placement that is the direct parameter of mask layout. So the layout parameters and the source parameters interfere to each other physically. This means co-optimization of source and mask layout has much freedom or potential of patterning. [3], [4]

2.3 Simulation condition

The exposure condition is as follows. The wavelength is 193nm. The NA=1.35. The illumination source is a cross pole. The intensity distribution is constant (flat) but the intensity of x and y pole is independent and tangential polarization is applied. Binary mask of dark field is used. Here aerial image simulation is applied. The optimization cost is the worst dose focus window of 12 holes measuring both x and y directions. We try getting solutions by single exposure.

3. OPTIMIZATION RESULT AT CENTERAL AREA OF MEMORY CELL BLOCK

3.1 Standard condition

Here we set a target to get circular image whose diameter is the mask size (40nm). The original design is the target. Figure 5 and 6 show the optimized source, layout, contour, and the process window. In this case we can get some process window by single exposure. Though we think the result is remarkable, the DOF (EL=5%) is as small as 30nm, which occurs at semi-isolated holes. It is not enough for production. We can also see a pattern shift shown in figure 6 with an arrow. The blue dots are both ends of the cut lines for evaluation and it means no shift that the contour of hole is placed in center of 4 dots of the x/y cut lines. We have to improve the process.

3.2 Oval holes

The patterns of contact layer are connected to the underlying layers whose shapes are rectangles that are longer in y-direction. So the contact pattern can be somewhat oval shape that is longer in y direction from viewpoint of device. From viewpoint of lithography, it is advantageous to make the illumination source more like x-dipole shape to resolve the minimum pitch of 90nm that exists in x direction while one in y direction is 106nm. This source tends to make holes oval in y direction. So it matches requirement of device and lithography to make the target CD in y-direction longer keeping one in x-direction same as the original target. Here we set the target of y length 55nm that is longer by the 15nm than the original. Figure 7 and 8 show the optimized source, layout, contour, and the process window. With this condition we can improve the DOF to be 47nm which is larger by the 17nm than the standard condition and we do not see any large pattern shift. The pattern shift caused by asymmetrical layout is suppressed by the shift of rectangular mask pattern which is determined by co-optimization. The improved resolution by applying oval shape makes it possible. The hole shown with an arrow in figure 8 is the typical case.

The optimized source has stronger intensity and wider opening angle of x-dipole than y-dipole. This is reasonable considering the minimum pitch exists in x direction. In case of target of circular shape the intensity distribution is
opposite. This means the condition does not match the lithographic characteristic. Considering this phenomenon it seems very effective to apply the target of oval shape.

3.3 Insert on SRAF

Seeing the layout there are several pitches in the block, which makes it harder for source to be specific to improve DOF. So we consider applying SRAF patterns. We have our original technology of creating SRAF patterns [5], [6], [7]. It calculates an approximate aerial image of 2D TCC calculation and the image is differentiated twice. SRAF patterns are created on peaks of the image considering mask fabrication constraints and preventing SRAF patterns from being printed.

We take procedure for co-optimization with SRAF pattern below. At first SRAF patterns are created on the original layout under the optimized source for oval shape. Figure 9 is the aerial image of 2D TCC calculation that is differentiated twice. Figure 10 shows the created SRAF patterns among the original pattern. Secondly co-optimization is applied to the patterns getting the target shape to be oval.

Figure 11 and 12 show the optimized source, layout, contour, and the process window. Here we can get DOF (EL=5%) of 84nm with no printing of SRAF. It is larger by the 37nm than the case of no SRAF with oval shapes. This DOF is quite enough for mass production. The outer $\sigma$ is 0.964. The ratio of inner / outer $\sigma$ is 0.799. The intensity and open angle for x-pole and y-pole are 1.00/90 degree and 0.44/38 degree, respectively. This source is more like x-dipole than one for case of oval shape without SRAF. It is reasonable. Since the pitches become more uniform, the strong x-dipole has been able to be applied to have better process latitude for the pattern with minimum pitch.

The mask layout consists of just simple rectangles. The source is just a cross pole with 2 intensities in x and y direction. The simple mask layout can reduce the mask cost and the simple source can be easily set in conventional exposure tools. It contributes to COO.

4. APPLICATION OF OPC

4.1 Dose focus window

To examine the lithography performance by the complicated mask pattern in contrast to simple mask pattern by our method, we apply conventional OPC to the original pattern with SRAF. The target shape is oval to get better result. Here we use mask pattern whose x and y sizes are the target CD of oval shape, because OPC tries to make the image contour to be the original mask counter. The source is the optimized one in case of getting oval shape using SRAF, because this condition has the best performance. Regarding OPC parameters the resolution or segment size is 5nm (on wafer) and the offset from corners is 10nm. Since we investigate theoretically, we do not consider the manufacturing ability of mask.

The OPC result is shown in figure13. The mask shape is very complicated. Here the mask patterns with no bias and +0.5nm bias are drawn and the corresponding contours are shown. The CD error (rms) is 2.5nm. Figure 14 and 15 show the layout applied OPC, the contour, and the process window. Though DOF (EL=5%) of 58 nm is got, it is less than the DOF of 84nm by co-optimization in spite of the complicated mask pattern. In figure 16 the summary of all DOFs that have been evaluated are shown. The co-optimization in case of oval shape and SRAF is the best.

4.2 Measurement of MEEF

Figure17 shows MEEF values of results of OPC and co-optimization. MEEF is determined by shifting the segmented mask edge by 0.5nm along the sides and measuring the CD deviation at the cut lines. This method corresponds to the actual fabrication of mask where the mask CD varies uniformly in area as small as the parts of the memory cell. As shown, every value of MEEF of co-optimization is lower than OPC. In addition the mask pattern by co-optimization is as simple as rectangles, so the mask fabrication becomes easy. Combining lower MEEF and easier fabrication, co-optimization result provides better CD control than conventional OPC technology.

4.3 Reason of reducing MEEF

Figure 18 shows NILS values of results of OPC and co-optimization. It proves NILS of co-optimization is just a little larger. So image by co-optimization does not seem drastically better than one by OPC. The superior MEEF of co-optimization cannot be explained by the image quality. Figure 19 shows MEEF of 4 patterns whose complexity varies from such a simple pattern of rectangle to such a complex pattern of complicated OPC. We can say that the complex patterns are, the higher MEFFs are. We suppose the mechanism as follows.
The increase of pattern area by shift for MEEF measurement is larger for case having more sides such as OPC patterns than for case having fewer sides such as rectangles. Generally speaking the increase of pattern area corresponds to the increase of energy onto wafer, which leads to more CD change or higher MEEF.

5. PIXEL ILLUMINATION SOURCE

5.1 Application of pixel illumination source

We apply pixel illumination source here. We use a technology of ‘Linear programming (LP)’. It has a characteristic of getting the strict solution that is proved mathematically right. Since in this method the mask layout is to be fixed, we use the mask layout optimized in condition of oval shape and SRAF insertion. The pixel counts 766. The optimization cost is the dose focus window that is same as the co-optimization. The optimized sources are shown in figure 20. The 3 ones from the left are pixel sources and the rightmost one is the source optimized by co-optimization as the reference. From the left to the right the 3 source becomes less discrete considering manufacturing ability of the source. The mathematical definition is how much smoothly intensity of a pixel changes from a pixel to a neighboring pixel. The DOF becomes smaller as being less discrete due to the restricted condition. The result is interesting. The DOFs by LP are almost same as one by co-optimization regardless of the strict solution, shown in figure 21. The source shape becomes similar to one by the co-optimization as it becomes less discrete. The least discrete source is almost same as one by co-optimization. It is rare that such a source as conventional shape is got under pixel based optimization. This means co-optimization can find a solution close to the strict solution by LP and the simple source by co-optimization is completely matched with the simple mask layout.

6. OPTIMIZATION RESULT CONSIDERING EDGES OF MEMORY CELL BLOCK AND THE ARRAY CIRCUIT BLOCK

6.1 Evaluated area

We have shown our co-optimization works well for the memory cell (MC) pattern, supposing the same layout is repeated endlessly. However there actually are edges of MC block. Since the edge area is adjoined the array block, the layout condition is different from the central area. So we have to consider the edge areas together with the central area.

For the purpose we choose 4 areas of MC as optimization targets that are located inside the MC block, at the intermediate position of lower edge of the MC block, at the intermediate position of right edge the MC block, and at lower right area of the MC block. It is shown in figure 22. The central area is the unit block used to optimize the MC pattern. Every area of MC has the same layout circumstance as one of above 4 areas. The 4 corners have the same layout circumstance and can be represented by the lower right area. The upper and lower edge areas of MC except the corners have the same layout circumstance and can be represented by the intermediate position of lower edge. The inside areas have the same layout circumstance and can be represented by the central area. Since the sizes of the edge areas are several 100 nm, 1 edge area from the boundary of MC block goes beyond the optical proximity effect. This means the inside areas neighboring the edge areas can be represented by the central area.

Regarding the array circuit area we choose 2 corner areas and 2 intermediate positions of the edge areas adjoining the right and lower edges of MC, adding an inside area of the array circuit below the MC block. It totals 5 areas. The entire array circuit area is represented by them.

Each 9 pattern is described individually by the layout parameters considering the layout symmetry and they are optimized simultaneously with the source parameters. The layout parameters count 532. It is numerous and the MEEF value is as high as 10. Though we use an optimization method of downhill simplex, the conventional method cannot get good solutions. So we incorporate a new idea that the mask parameters are more often and more carefully optimized in SMO considering that the mask parameters impact on optimization far more than the illumination one. As a result we can find the good solution without being trapped at bad local solutions.

6.2 Optimized result

The optimized result of the worst 9 patterns is shown in figure 23. DOF (EL=5%) of 58 nm is achieved by single exposure. Everything is a location of the array circuit. This DOF is almost enough for production and can be improved by some layout modification, since the bottle neck is the array circuit. In figure 24 they are shown.
In actual chip we propose that this type of co-optimization is applied to MC block considering the boundary area, and the array circuit and the peripheral circuit are applied such a mask optimization as OPC under this optimized source. The source is applied to the full chip. It is hard to determine the optimum source for numerous patterns in the full chip, and MC and the array circuit patterns are the hardest patterns to resolve. So the source optimized here is appropriate as the representative for the full chip.

7. CONCLUSIONS

Co-optimization technique can make it possible for 20nm node SRAM contact layer to be fabricated with process latitude by single exposure method. Co-optimization technique can optimize the entire memory cell block including the array circuit with the robust optimization engine.

The lithographic performance is better than conventional OPC and might be better than SMO that iterates source optimization and OPC. Especially MEEF is far better, which leads to an advantage of CD accuracy together with easy fabrication of mask. This result can be achieved by binary masks with simple patterns and simple source shape. They contribute to better COO.

Lithography began with simple technology and it has entered the world using advanced but complicated technology including expensive tools and material. However applying our co-optimization technique together with litho-friendly design we can be back to the world using simple and inexpensive technology.

REFERENCES

Figure 1.
Layout of contact layer of 20nm node SRAM. The layout has a basic block. The boundary is shown by rectangles.

Figure 2.
Each hole in the basic block is classified to groups with same circumstance of position according to the symmetry. The holes with the same circumstance are painted the same color. The number is index of each group.

Figure 3.
Layout parameters of the length of sides (x, y) and the position deviation from the original design (dx, dy). The dotted rectangle is the original design.

Figure 4.
6 illumination source parameters. The intensity of each pole is constant.

Figure 5.
The process window in case that the CD target is 40nm for both of x and y direction and the optimized source are shown. The DOF (5%EL) is 30nm.

Figure 6.
The optimized layout (green rectangles) and the image contours at best focus (red) and 50nm defocus (blue) in case that the CD target is 40nm for both of x and y direction are shown. The blue dots are both ends of the cut lines for evaluation.
Figure 7. The process window in case that the CD targets are 40nm and 55nm for x and y direction respectively and the optimized source are shown. The DOF (5%EL) is 47nm.

Figure 8. The optimized layout (green rectangles) and the image contours at best focus (red) and 50nm defocus (blue) in case that the CD targets are 40nm and 55nm for x and y direction respectively.

Figure 9. The aerial image of 2D TCC calculation that is differentiated twice.

Figure 10. The created SRAF patterns (red) among the original patterns (blue).

Figure 11. The process window in case of applying SRAF and the optimized source are shown. The CD targets are 40nm and 55nm for x and y direction respectively. The DOF (5%EL) is 84nm.

Figure 12. The optimized layout (green rectangles) and the image contours at best focus (red) and 50nm defocus (blue) in case that the CD targets are 40nm and 55nm for x and y direction respectively.
Figure 13.
The layout that is applied
OPC and the image contours
with no bias and +0.5nm
bias. The right figure is
zoomed in.

Figure 14.
The process window in case of applying OPC
on the original layout with SRAF is shown. The
CD target is oval. The DOF (5%EL) is 58nm

Figure 15.
The layout applied OPC
(green rectangles) and the
image contours at best
focus(red) and 50nm
defocus(blue) in case that
the CD target is oval. The
SRAF patterns are colored
purple.

Figure 16.
The summary of DOFs of 3
results of co-optimization and an
OPC result. The image contours
at best focus(red) and 50nm
defocus(blue) are shown.
Figure 17. MEEF at every hole.

Figure 18. NILS at every hole.

Figure 19. MEEF of a mask pattern by co-optimization and 3 types of OPC patterns. The mask bias shift is 0.5nm.

Figure 20. The 3 sources from the left (a,b,c) are ones optimized by LP. The rightmost one is the one optimized by co-optimization.

Figure 21. Each DOF of each optimized source (a, b, c, d) in figure 20.
Figure 22. (Left)
Areas to optimize the entire memory cell block and the array circuit block that consists of 4 areas in memory cell block and 5 areas in the array circuit block.

Figure 23. (Below)
The process window considering the entire SRAM which consists of memory cell block and array circuit block is shown. The CD targets are 40nm and 55nm for x and y direction respectively. The data of the worst 9 locations are shown. The DOF (5%EL) is 58nm.

Figure 24.
The worst 9 patterns are shown. Everyone is located in the array circuit block.