

Optical lithography applied to 20nm CMOS Logic and SRAM

V. Axelrad, Sequoia Design Systems, Inc. (United States);

M. C. Smayling, Tela Innovations, Inc. (United States);

K. Tsujita, K. Takahashi, Canon Inc. (Japan)

Abstract

Achieving 20nm designs with 193nm lithography is difficult even with immersion technology. At 20nm, the metal-1 pitch will be ~64nm, which is well below the 80nm limit for single exposure. In this work we extend on our earlier results [1-4] to show simulation-based patterning of both SRAMs and logic cells. This is consistent with the emerging industry consensus that regular designs and multiple exposure techniques will extend 193nm immersion as far down as 7nm [5].

The approach relies on 1D Gridded Design Rules with Lines/Cuts (1D GDR LC) selective double patterning. Due to the highly regular patterns of 1D GDR LC we are able to determine a sharp lithographic optimum as a result of numerical co-optimization of key layout parameters and lithography settings such as scanner illumination, etc. including realistic scanner capability.

Critical layers (holes/cuts in 1D GDR LC) consist of a number of identical hole/cut patterns with varying density. We propose a novel algorithm for full-chip proximity correction of such critical layers. The algorithm consists of 1) a source-mask optimization step (SMO) to choose optimal scanner settings for a class of designs using standard cells, followed by 2) a final correction step applied to the entire layout to determine individual sizing for each cut to compensate for its optical/process environment. This procedure converges rapidly in our test cases producing close to 0nm CD error for each cut. Several test designs including one with approximately 100k transistors using ~20 cells from a standard cell library including both SRAM and logic cells were used, with good convergence obtained in all cases.

Our procedure is a combination of an SMO step followed by cuts-OPC, the equivalent to OPC applied to cuts of 1D GDR LC designs. The procedure scales linearly with layout area and can be efficiently applied to full-chip designs.

Co-Optimization of Layout and Lithography (SMO - Step 1)

Simultaneous optimization of layout patterns and lithography settings (source-mask optimization - SMO) is made possible by the uniformity and repeatability of the lines/cuts patterns (Fig. 1, Fig. 2). We use direct optimization and experimentally validated lithography simulation for the critical cuts layers. Optimization variables are:

- cuts geometry (width, height, hammer heads) (Fig. 3 shows the layout parameters and simulated cut pattern)
- illumination of the scanner lens entrance pupil (Fig. 4 shows the optimized illumination)

The optimization cost function is RMS CD error (actualCD - targetCD) across all cuts. Minimizing this cost function also reduces variation among cuts by getting all CDs close to the same target value. To make sure that sufficient overlap between lines and cuts is produced, multiple cutlines (CD measurement locations) are used for each cut pattern as shown in Fig. 3.

To ensure a sharp optimum as well as fast calculation SMO is performed using one or several small sample portion(s) of the design, typically 4 μ m \times 4 μ m or smaller. Due to the regular nature of 1D GDR standard cells we observed excellent stability of SMO results across randomly picked sample locations (Fig. 5). The optimal illuminator shape for our design with horizontal cuts is a horizontal dipole. This illumination produces a small CD error in the horizontal direction and an oval vertically elongated shape (see Fig. 3) for better cuts/lines overlap coverage and yield.

Cuts-OPC - local layout correction of cuts to compensate for optical proximity effects (cuts-OPC - Step 2)

After completion of Step 1 we process the entire design in overlapping windows of convenient size, typically 4 μ m \times 4 μ m or 6 μ m \times 6 μ m. Using global parameters (width, height, hammerheads + scanner illumination), a simulation is performed, CDs at each cut are extracted and individual biasing of each cut is adjusted iteratively to minimize RMS CD error (actualCD - targetCD at each cut). Typical convergence behavior is shown in Fig. 6, in general 3-5 iterations are sufficient to reduce CD RMS error to <1nm. Simulation time for one such window is around 30-60 secs on a quad-core machine

Application: 100k Transistor 20nm Standard Cell Design with SRAM and Logic Cells

A test design with about 100k transistors was used to validate the procedure. The design used 20nm standard cells including both SRAM and logic 1D GDR cells. Uniformity of Step 1 results - optimal scanner illumination - across randomly picked sample areas from our design demonstrate good pattern uniformity in different library cells. With this SMO result we then proceed to Step 2 - cutsOPC - to adjust individual sizing for each cut in the design. As mentioned above, this is done in overlapping windows, which are independent from each other and can be processed simultaneously on different CPUs. For each one of these windows we saw rapid convergence with <5 iterations required for <1nm CD RMS error. Post-correction M1 cut patterns are shown in Fig. 7, all CDs are on target. CD and bias (correction) histograms for all 1D GDR cuts are shown in Fig. 8. Biases applied to each cut provide some information about the necessary level of layout modification. Bias outliers can be therefore be used to flag more difficult locations of the design to identify where design changed may be needed.

Results and Conclusions

A novel procedure for full-chip correction of proximity effects in 1D GDR LC standard cell designs was presented. The procedure includes an SMO step to determine the optimal scanner settings and a cuts-OPC step to choose optimal layout parameters for each individual cut pattern. The procedure converges well for 20nm design rules and produces on-target (0nm CD error) cut patterns. Several test designs were used to validate the approach including a 100k transistor design with SRAM and logic cells. Good convergence was achieved for all library cells in their specific optical environments. The procedure is fast, scales linearly with layout area and is well applicable to full-chip designs.

References

- [1] V. Axelrad, M. Smayling, "16nm with 193nm Immersion Lithography and Double Exposure," SPIE, 2010.
- [2] K. Tsujita, K. Mikami, J. Ishii, T. Arai, K. Takahashi, "Lithography and layout co-optimization beyond conventional OPC concept," SPIE, 2010
- [3] M. Smayling, V. Axelrad, "Simulation-Based Lithography Optimization for Logic Circuits at 22nm and below," SISPAD, 2009
- [4] M. Smayling, V. Axelrad, "32nm and below Logic Patterning using Optimized Illumination and Double Patterning," SPIE, 2009
- [5] Y. Borodovsky, "Lithography 2009: Overview of Opportunities," Semicon West, 2009

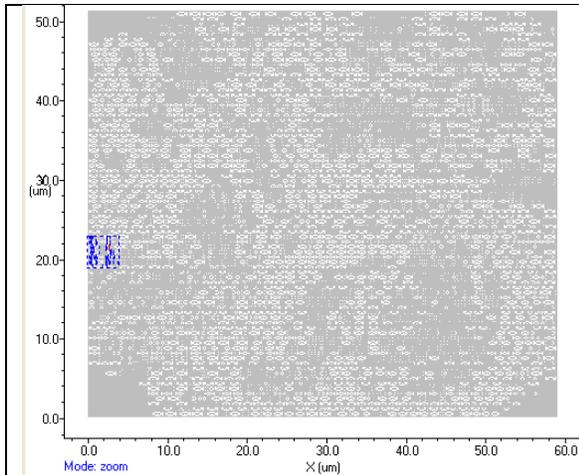


Fig. 1 Floor plan of the test design using 20nm standard cells, total area 50 μ m \times 60 μ m, each box is a standard cell, one of the windows used for cutsOPC (Step2) is highlighted.

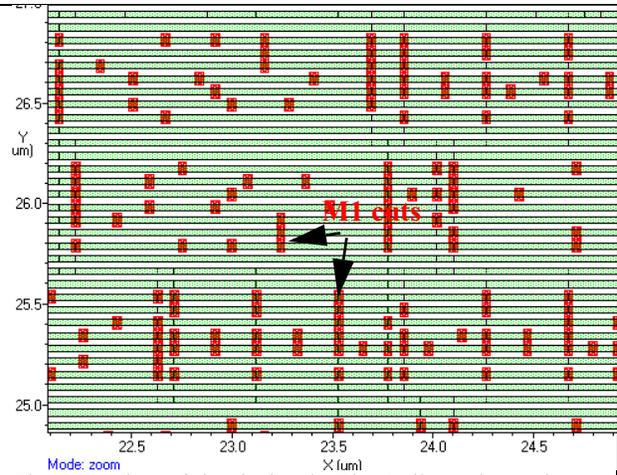


Fig. 2 Portion of the design in Fig. 1, lines shown in green, cuts in red. Multiple standard cells can be seen in this view with different configurations of cuts.

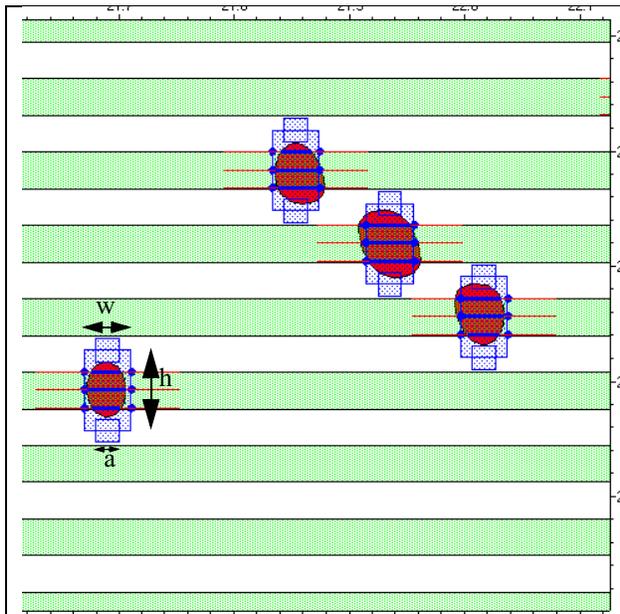


Fig. 3 Parameters used to adjust the shape of each cut: height h , width w and hammerhead a are global (same for all cuts) and optimized in Step 1 together with illumination (source), the size of each cut is then individually adjusted by a bias parameter (one for each cut) in Step 2 - cutsOPC.

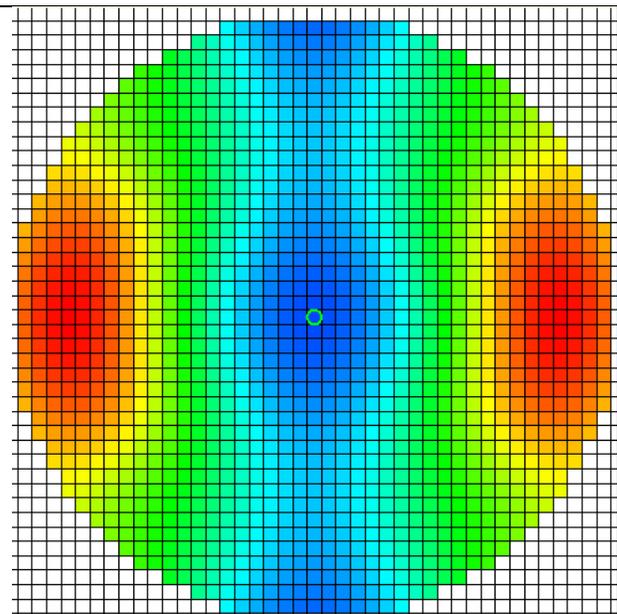


Fig. 4 Optimal scanner illumination obtained by simultaneous optimization of cut shape parameters shown in Fig. 3 and scanner illumination in Step 1.

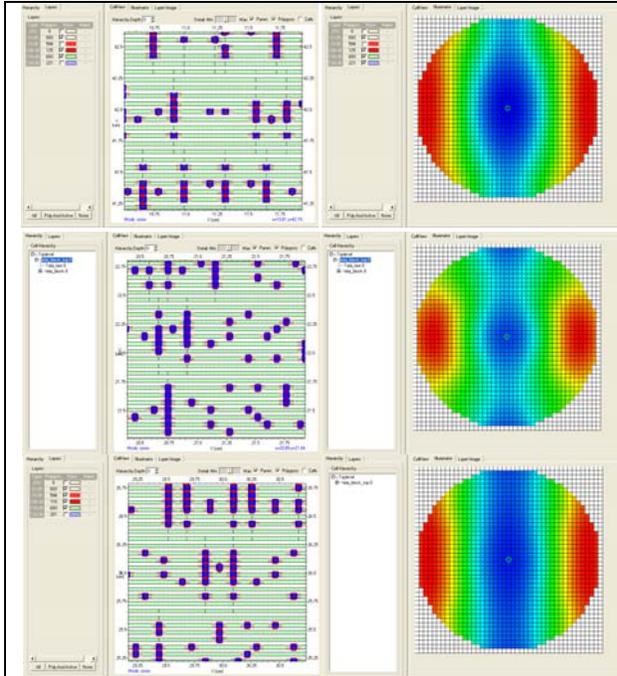


Fig. 5 SMO results (Step 1) across randomly picked sample locations, each one is $3\mu\text{m} \times 3\mu\text{m}$: optimal illumination and a portion of M1 cut patterns. Top: sample 2 at $x=10, y=40$, middle: sample 1 at $x=20, y=20$, bottom: sample 0 at $x=28, y=24$.

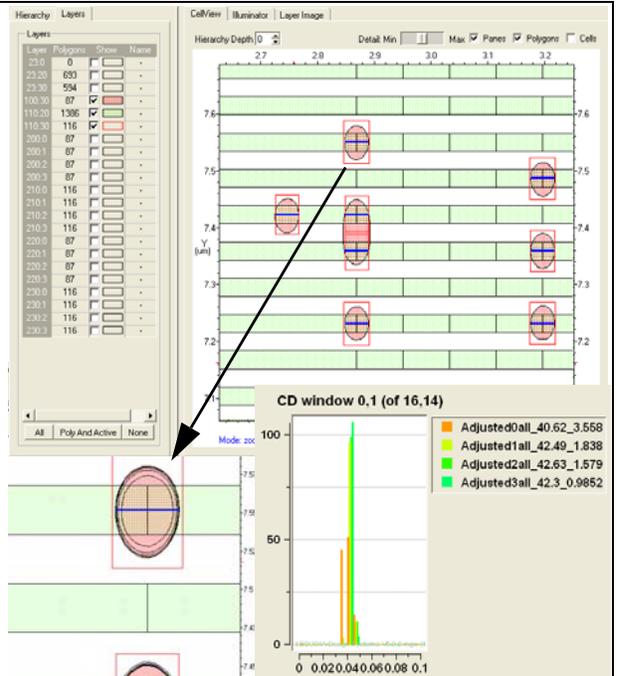


Fig. 6 Convergence behavior of cutsOPC - iterative pattern correction to get cut CDs on target. Top: view of several post-correction cut patterns, all CDs are on target; bottom right: CD histograms during the iteration, final CD sigma is 0.98nm; bottom left: successive cut patterns during the iteration.

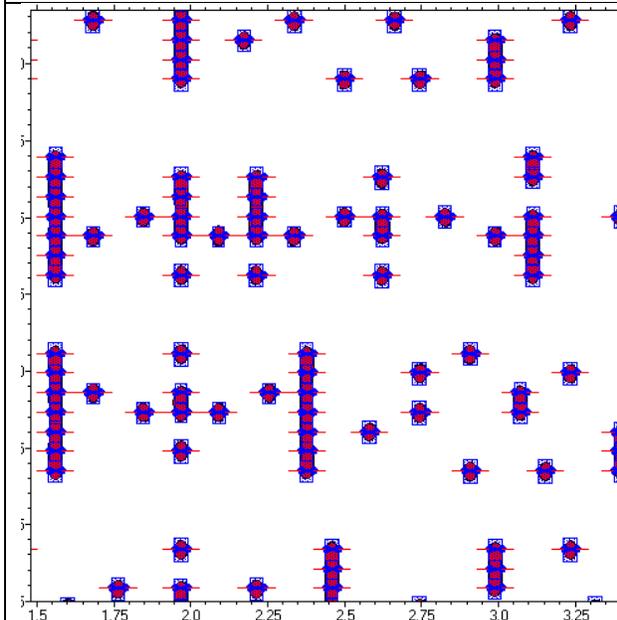


Fig. 7 Post-correction M1 cuts and cutlines used to measure and adjust the layout. All cuts have on-target CDs irrespective of their optical environment.

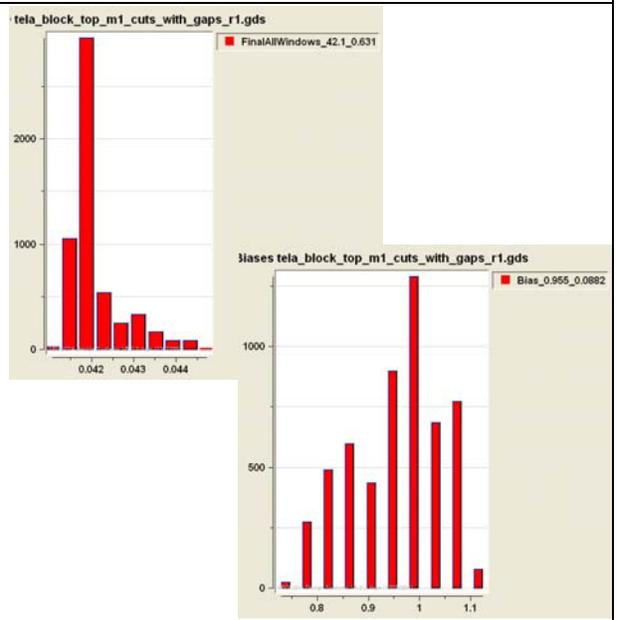


Fig. 8 Histograms of post-correction CDs and biases used to correct individual M1 cut patterns. Sigma CD = 0.6nm, Sigma Bias= 9%.