Gridded Design Rules – 1-D Approach Enables Scaling of CMOS Logic

One-dimensional (1-D) gridded design rule (GDR) cells have demonstrated a number of advantages over 2-D complex design rule (CDR) cells, including smaller area, better gate CD control, and elimination of hotspots. Because of their regularity, 1-D GDR-style cells are expected to scale to 32nm with single pass exposure using optimized exposure conditions.

Keywords: Gridded Design Rules, SADP, CD Control

The semiconductor industry has benefited from the relatively straightforward lateral and vertical scaling of integrated circuit dimensions for the past 50 years. The main challenges of each new technology node have been in the photolithography and device/interconnect processing steps. However, for the randomly-arranged logic circuits used in CMOS system-on-chip (SOC) devices, a paradigm shift in design style is required to permit continued scaling. GDR-LC, which uses a "line" plus "cut" approach is proposed as a design solution. Combined with a spatial frequency multiplying technique such as self-aligned double patterning (SADP) and a sparse pattern exposure approach such as multiple e-beam (MEB), GDR-LC should allow continued scaling to the 16nm logic node and beyond. GDR can also be applied to older logic nodes to reduce die cost.

The continual improvements in photolithography resolution have enabled the dramatic scaling of IC feature sizes. The k_1 factor is used in the Rayleigh equation as:

$$CD = k_1 \bullet \frac{\lambda}{NA}$$

where *CD* is the critical dimension or minimum feature size, λ is the wavelength of light used in the stepper and *NA* is the numerical aperture of the stepper lens as seen from the wafer.

In spite of improvements in the optical source related to the photon wavelength, and concurrent improvements in numerical aperture, the k_1 value has been on a downward trend for several technology nodes. With λ/NA limited to 143nm, low k_1 will continue to be the focus for reducing feature sizes.

If we examine the trend in k_1 for logic technology nodes extending from 180nm to 16nm, wavelengths are 248nm for the KrF excimer laser, 193nm for the ArF excimer laser, 133nm for water-immersion ArF, and 13.5nm for soft x-rays or EUV. NAs range from 0.25 to 1.35 and different combinations of increasing NA, decreasing wavelength, immersion, and double patterning are available. At 22nm, the k_1 value is below the theoretical minimum of 0.25, illustrating the requirement for double patterning.

Until the 45nm node, the choice of a cost-effective lithography solution was fairly consistent across the industry. Each node had a higher lithography cost, but the area reduction from scaling also lowered die cost. The decrease in k_1 was accommodated by the increased use of resolution enhancement techniques (RETs)

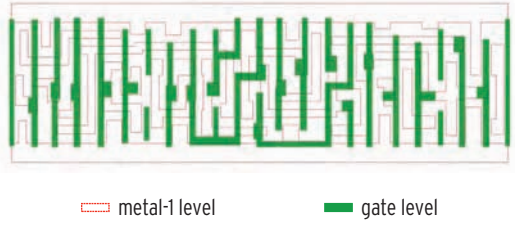

Figure 1a. Two dimensional logic cell layout.

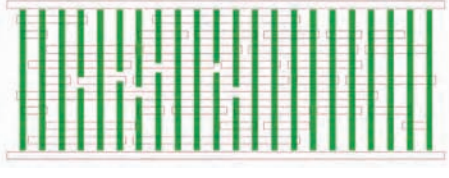

Figure 1b. One dimensional cell layout.

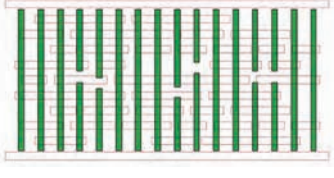

Figure 1c. Another one dimensional logic cell layout.

such as attenuated phase shift masks (att-PSM), off-axis illumination, and optical proximity correction (OPC).

At the 45nm node, two approaches are being taken. One, using dry lithography, requires a change in design style to a more 1-D physical layout with straight lines. The other, using immersion lithography, allows a conventional 2-D design style with bends, but with many complex design rules.

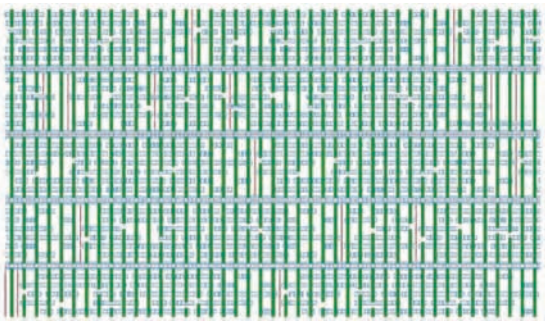

Figure 2. Portion of a logic block after place and route showing the regularity of 1-D GDR.

Design Styles

A partial physical layout of a commonly used logic standard cell, the scan-D flip-flop (SDFF), is shown in Figures 1a and 1b. Another functional logic cell is shown in Figure 1c. The solid green polygons are the gate level, and the dashed outline red polygons are the metal-1 level. Figure 1a shows the conventional 2-D layout style, in which lines are drawn with bends and have multiple pitches. Figure 1b shows the Tela Canvas™ 1-D GDR layout style, in which the lines on each level are straight, without bends, and on a fixed pitch. The orthogonal gate and metal-1 lines define an x-y grid which is propagated throughout a block of logic cells.

The appearance of the layouts in 1b and 1c is virtually the same, even though the logic functions are completely different. This uniformity of layout patterns, independent of logic function, is a critical factor in the benefits of the 1-D GDR layout style. Figure 2 shows a portion of a logic block after standard cells have been placed and routed. The uniform vertical gate lines and horizontal metal-1 lines make the overall block extremely regular.

The conventional 2-D design style has been used since the beginnings of logic IC design. For recent technology nodes, the number of design rules per mask layer has doubled from 180nm to 45nm. The percentage of "complex" design rules, i.e. rules with multiple dependencies or restrictions, has increased from ~20% to >60% of the rules during the same period.[1,2,3,4] The additional rules, and the complexity of the rules, are directly related to the problem of patterning 2-D shapes with lower and lower k_1 lithography.

Because of the lower fidelity of the lithography process at advanced technology nodes, attempts have been made to produce design with acceptable yields using design rule check (DRC) tools. Additional rules, variously named restricted or radical design rules (RDRs), have been added to existing rule decks to help designers address the pattern fidelity problem.[5] Additional efforts have been made to systematically create layout patterns, then evaluate them in simulation and patterned wafers to develop restrictions on allowed combinations of shapes, sizes, and spaces.[6]

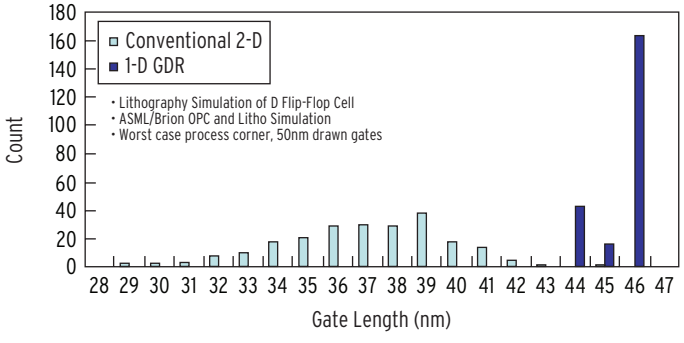

Figure 3. Gate CD distribution for 1-D and 2-D layout styles under worst-case simulated exposure process.

A change in design style was demonstrated by Intel in its 45nm CMOS process in which dry lithography was used to reduce cost and risk.[7] This resulted in a lower k_1 value than if immersion lithography had been selected. To maintain pattern fidelity, the design style was 1-D for critical layers like the gate. One benefit of the regular layout style was a 37% reduction in number of logic rules for 45nm compared to 65nm. The benefits of regular layout styles have been discussed by other groups as well.[8]

Another feature of the Intel 45nm process was the use of lines and cuts for the gate level. The 1-D features were formed from long lines that were selectively cut using a second photomask – resulting in the final gate shapes on a wafer. This approach improves gate CD control and reduces the line-end overlap for contacts and the overhang of transistor channels. The logic and SRAM layouts have unlanded gate contacts, i.e. those where the contact does not completely sit on the active area, further improving the CD uniformity.

1-D vs. 2-D Comparison

We compared 1-D GDR layouts to 2-D CDR layouts for several circuit designs at technology nodes from 90nm to 45nm. In each case, the 1-D cells were 5-17% smaller than the conventional 2-D cells for allowed design rules. This is a significant area improvement that

translates directly into cost and yield improvements.

Improved CD Uniformity

The most critical process parameter in a CMOS technology is the gate electrode linewidth, often called gate CD. Historically, through the impact on transistor saturation current, gate CD was controlled to keep product speed distributions within a yielding range. More recently, with transistor scaling halted by the atomic limits of the gate dielectric thickness, transistor sub-threshold leakage has become another reason for improving gate CD uniformity.

Gate CD uniformity can be split into three components: wafer-to-wafer, within-wafer, and within-die. Wafer-to-wafer uniformity is improved by using advanced process control (APC) in process equipment such as that employed by the Applied Centura AdvantEdge Silicon Etch system. This system makes gate CD measurements on each wafer, then trims the resist or advanced patterning film (APF) to center the resist CD on target. Within-wafer and within-die gate CD can be improved by die-to-die exposure compensation and by optimizing the etch reactor configuration and process conditions. Within-wafer etch CD uniformity and etch microloading, which affects within-die uniformity, may be challenging to optimize simultaneously. By contrast, a regular circuit layout pattern with uniform density such as that produced using the Tela Canvas application is expected to reduce within-wafer non-uniformity by ~50% because it is no longer necessary to optimize for microloading.

The greater impact of 1-D GDR on gate CD uniformity is on the within-die component. Figure 3 shows the gate CD distribution for both 1-D and 2-D logic cells under worst-case simulated exposure conditions. As in real, i.e. non-ideal optical lithography, although the drawn gate length is 50nm, the final CDs are shorter. The 1-D case maintains a tight distribution, whereas the 2-D case has a broad distribution with greater CD loss. Besides being a reliability concern, shorter gate lengths also create higher sub-threshold leakage currents. We measured the 1-D leakage to be 50% smaller compared to 2-D leakage on a 45nm test device.

Using aerial image simulations, gate CD was compared for six different logic cells and four different layout styles/environ-

How Gridded Design Works

Process engineers have a three dimensional view of the chip through cross-section and top-down SEMs. Design engineers only have a top-down view, which they create in a layout editor. The layout is built up with multiple levels, which represent the masking layers to be used in the wafer fab.

A portion of a conventional layout is show in Figure S-1 (left) for a 2-D design style. 2-D in this case refers to shapes on the same level that can be oriented in the x or y direction, or bent to have sections aligned in both x and y. Because of the bends and jogs, complex design rules are needed to communicate processing limitations from the fab to the designers. The additional complexity in the rules has also been described as restricted design rules (RDR).

The figure shows three problem areas in the layout. ① is a gate line which is isolated and will have a different process window than a gate line surrounded by a more dense array of lines; ② shows a gate in a dense pattern, but the pitch is different on each side of the line, again causing a reduced process window; ③ shows a congested region with bent gate shapes that require additional design rules and also reduce the process window.

Figure S-1 (right) shows a similar portion of a layout, but in this case 1-D GDR is used. 1-D refers to shapes on critical levels without bends or jogs. "Gridded" refers to a fixed pitch used for shapes in the x and y directions (not necessarily the same pitch in x and y). With the gate and metal-1 levels on a grid, the contacts between them also fall onto a grid. GDRs become very simple, since there are no 2-D shapes to deal with.

Once a layout is done in the 1-D GDR style, it becomes straightforward to build the line segments by patterning longer lines on grid, then cutting the lines to form the segments using a second photomask. This 1-D GDR-LC approach allows the use of less advanced lithography tools for the lines. The same lithography tools can then be used for the cuts to form the hole patterns for contacts and vias.

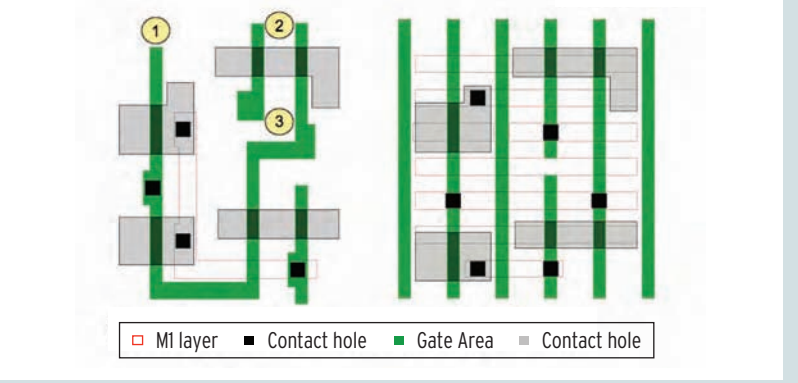

Figure S-1. (Left) 2-D complex design rule layout and (right) 1-D gridded design rule layout.

CoV (%)	2-D self	2-D simple	2-D complex	1-D self
Cell F	7.0	7.0	7.0	0.2
Cell E	1.2	1.1	1.2	0.3
Cell D	0.9	0.8	0.9	0.4
Cell C	0.9	0.8	1.0	0.1
Cell B	16.0	16.2	16.3	0.1
Cell A	7.2	7.2	7.1	0.4

Table 1. Aerial image simulation of gate CD for various layouts shows consistently low coefficient of variation for 1-D patterns.

ments. Aerial image simulation follows the same steps as in the physical world: The DRC deck is applied to a circuit design to ensure manufacturability as far as possible. OPC features are then applied and the aerial optical simulation is peformed on the resulting pattern. The fidelity of the resulting aerial image is expressed by the dimensionless coefficient of variation (CoV), which is given by the ratio of the standard deviation from the mean CD to the mean CD:

$$CoV = \frac{\sigma_{CD}}{CD}$$

Table 1 summarizes the gate CD CoV results for the different layouts. The 2-D columns are for cells with different surrounding cells. "Self" means that the surrounding cells have the same layout as the cell being measured. "Simple" means that the surrounding cells are less complex and is essentially the case for which the image would be of the highest fidelity. By contrast, "complex" is the most difficult to image, with more complex cells surrounding the cell being measured. The 1-D column has the 6 cells surrounded by the same 1-D cell. For the 2-D cases, almost independent of surrounding layout context, the CoV ranged from about 1% to over 15%. For the 1-D case, all cells had a CoV of less than 0.5%. The 1-D GDR cells have a significantly better gate CD uniformity than any of the 2-D cells.[9]

The cells evaluated for Table 1 were in relatively small layout blocks, with three rows of cells and three to four columns of cells. In order to pose a more severe test for the 1-D layout, a larger, more representative block of cells was constructed and simulated to get aerial image contours. The CoV results for a 270µm wide by 250µm tall block are shown in Figure 4. Each point represents the CoV for a group of cells in that row of the standard cell block. The cell groups and their placement in the block represent all the permutations of a group of ~300 standard cells in a 45nm library. We were unable to determine any systematic special correlation in the data, indicating that the gate CD uniformity is relatively independent of context and in the worst cases still very small compared to 2-D results.

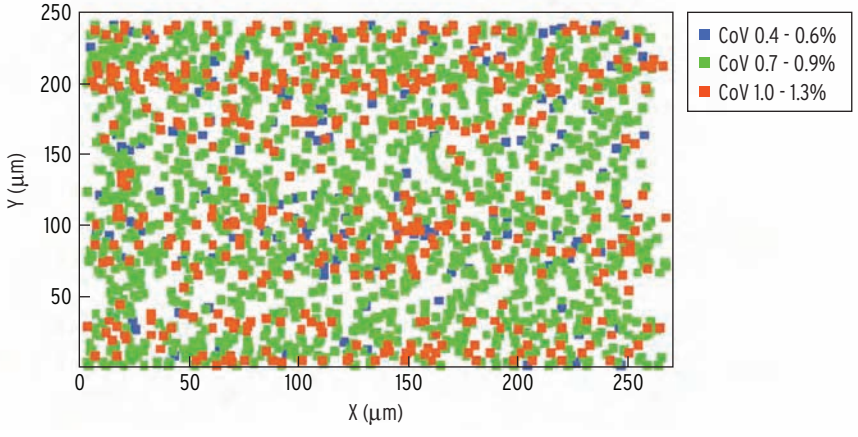

Figure 4. Gate CD uniformity for a logic block generated using aerial image simulation.

Improved Hotspot Prediction

Another criterion for logic cell quality is the number of hotspots, or regions in the aerial image of the layout that may have narrow linewidths (necking) or small inter-line spaces (bridging). Hotspot checking tools have become widely used at the 65nm logic node and below in order to improve yield by early identification of potential failing sites. Unfortunately, the hotspot checking is normally done on a finished block or chip, since 2-D layouts are sensitive to the context of surrounding cells.

The SDFF cell metal-1 layer was evaluated with the ASML-Brion simulation tool for hotspots. The results for a 7x10 design space, i.e. all combinations of 7 pitches and 10 end-gaps, are shown in Figure 5. In this plot, the x-axis is the end-gap in the metal-1, while the y-axis is the metal-1 pitch with approximately equal width and space. Several key points are shown in this figure. First, the 2-D version of the cell, drawn at the design rules and passing the DRC, had several hotspots, indicating that the DRC failed to predict layout flaws that would result in non-functional devices. These would have to be evaluated and potentially corrected after place and route, slowing down the design flow. The result of this uncertainty is that more relaxed design rules are often used to attempt to avoid

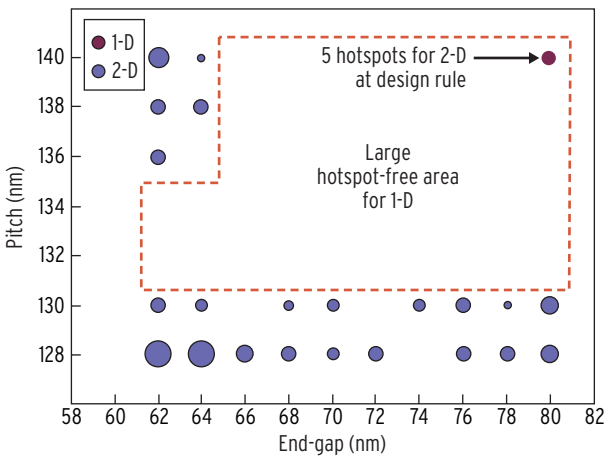

Figure 5. Metal-1 bridging hotspots. The diameter of the data point indicates the number of hotspots detected.

manufacturability problems, despite wasting 10% or more of the die area.

The second key factor illustrated by Figure 5 is that the 1-D cell layout could be generated for seventy (7x10) points in the design space, and there is a large region in which there are no bridging hotspots. These results show that a 1-D GDR cell can be evaluated over a large region of design space, and smaller rules could be used with better quality results compared to a 2-D cell. Given the uniformity of the GDR layout, the hotspot results are expected to extend across blocks of logic cells, meaning that hotspot checking can take place entirely at the design stage.

The ability to create and analyze design spaces should not be underestimated. The evaluation of such design spaces will allow faster development of design rules and more confidence that rules selected have a known margin from yield problems. This permits logic cell development to be more like SRAM cell development, which can be carried out concurrently with the process stabilization.

The scalability of 1-D GDR should be clear, given the lithography k_1 trend and the uniformity and hotspot results presented. Optimization of patterning conditions, such as the use of dipole illumination, will allow single pass patterning to be used for the 32nm node.

The 1-D GDR design style allows the use of lines and cuts to extend beyond single pass optical lithography. Logic nodes at 22nm and below will use the GDR-LC approach for logic and memories in SOCs. Pitch-halving by LELE (litho-etch-litho-etch) or SADP can form the lines at pitches for 16nm logic.[10] The cut patterns can be done with whatever lithography process is used for the contact and via hole patterns. Options include optical lithography with source-mask-optimization (SMO) and direct write e-beam. Because cuts are effectively 2-D structures, multiple e-beam (MEB) tools may be required for contact hole cuts at 22nm, replacing the optical cut mask. At low, 3-6% effective pattern density, an MEB tool is expected to be able to process 30-40 wafers per hour, keeping pace with an immersion lithography scanner.

The GDR-LC approach can be extended into the interconnect layers of an SOC. The design style can be applied to both orthogonal Manhattan layouts and X diagonal layouts.[11]

Conclusion

1-D GDR cells have been shown to have a number of advantages over 2-D CDR cells, including smaller area, better gate CD control, and elimination of hotspots. Because of their regularity, 1-D GDR style cells are expected to scale to 32nm with single pass exposure using optimized exposure conditions. Further scaling to 22nm and below can be achieved by combining GDR-LC with pitch-halving for lines and MEB for cuts and holes.

Acknowledgments

The author wishes to thank the Tela engineering and executive teams, especially Jon Quandt and Daryl Fox for creation of the cell design space and the large block with an exhaustive permutations of cells. The lithography simulations by Hua-Yu Liu and Lynn Cai of ASML-Brion were especially helpful for cell evaluations.

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