APF Pitch-Halving for 22nm Logic Cells using Gridded Design Rules

The 22nm Logic technology node, with line/space dimensions of ~32nm at a pitch of ~64 to 70nm, will be the first node to require some form of pitch-halving. Even with 1.35NA immersion scanners, the Rayleigh k_1 factor is below 0.25. A unique combination of an APF-based process sequence and a GDR-based design style permits implementation of random logic functions with regular layout patterns.

The APF (Advanced Patterning Film) pitch-halving approach involves using dual layers of APF both as the original full-pitch "form" as well as the hard mask at the half-pitch. APF is well suited for both because of its LER (Line Edge Roughness) reduction benefits and its simple deposition and etch characteristics.[1]

The process sequence involves patterning APF lines at the full pitch, then creating sidewall filaments of nitride. When the original APF is removed, the nitride lines are left at half of the original pitch. These lines are replicated into the second APF film, and then breaks in the lines are formed to separate segments of the lines based on circuit functions. The final material, for example a gate electrode, is etched as in a normal process.[2]

Figure 1a shows an SEM of lines after the pitch-halving process sequence. The 32nm line/space array shows excellent CD control and LER.

Figure 1b shows the layout of the "break" pattern to be used to cut the line array in the next pattern/etch step. Note that the breaks are like a contact pattern, but with elongated openings. Because the pitch of the breaks is not as tight as for the line pattern, the breaks can be patterned with conventional lithography and shrunk to size by a process like SAFIER.

The Tela Canvas implements GDR using strictly one-directional lines for the gate, metal 1, and metal 2 levels. These lines are placed on a grid, giving a grating-like layout which can be patterned at tighter design rules than conventional "random" layout. Because of the grating-like layout, random logic functions can be implemented using APF-based pitch-halving.

1. Wei Lie *et al*, "Method for fabricating a gate structure of a field effect transistor," US Patent 6924191, 2005.
2. Chris Bencher et al, "Self-Aligned Pitch Reduction, Applied Materials ET Conference, May 2007.
3. Michael Smayling, "Cell-based aerial image analysis of design styles for 45 nanometer generation logic," SPIE Microlithography 2007, Santa Clara, USA.

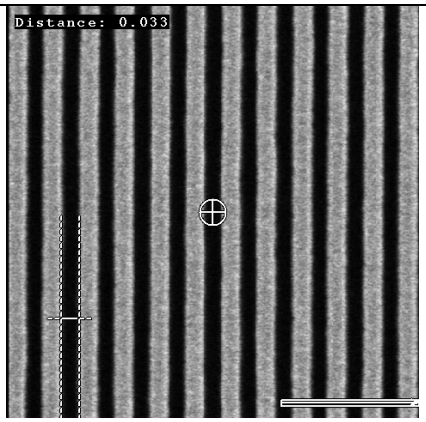

Figure 1a. Example of 32nm line/space array.

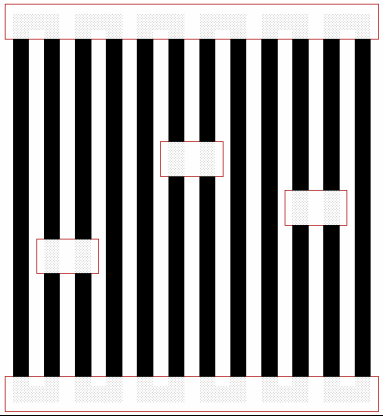

Figure 1b. Layout of a typical "break" pattern.