DFM – IT'S ALL ABOUT FLEXIBILITY

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ABSTRACT

The semiconductor industry has made great progress during the past 50 years, loosely following a trend described as Moore's Law in a continual drive for lower cost per function. Design for Manufacturability (DFM) has been an integral part of sustaining the trend, contrary to the belief that DFM was recently invented by a horde of EDA startups. The necessity for true DFM is discussed in the context of the current industry move to the 45nm logic technology node. Photolithographic fidelity, limited by the cost and availability of advanced scanners, requires extensive post-design processing or drives a change in design style.

INTRODUCTION

Progress in integrated circuit technology is often associated with scaling of lateral features. These features have gone from mils to microns to nanometers, giving an exponential increase in aerial density of functional elements like memory cells or logic gates.

A key factor driving scaling has been product cost. With device density increases from scaling, a circuit designer could choose between adding functions at a relatively fixed die cost, or reducing chip cost by keeping the function the same and just shrinking to get a smaller die size. Either way, the scaled chips often benefited from frequency increases and/or power dissipation decreases.

The golden days of scaling came to an end in the early years of this millennium.[1] A critical chip dimension, the thickness of the MOS transistor gate oxide, crashed into two realities: atoms have a finite size, and electrons can directly tunnel through thin barriers. This limited the power supply voltage scaling, which set the stage for the power dissipation crisis we face today.

Another factor impacting scaling is lithography. Starting with the 180nm logic technology node, critical levels entered the "sub-wavelength" era in which the features being patterned are smaller than the wavelength of the illumination light source. As illustrated in Figure 1, the gap between the wavelength (lambda or λ) and critical dimensions (CD) is widening for each successive technology node.

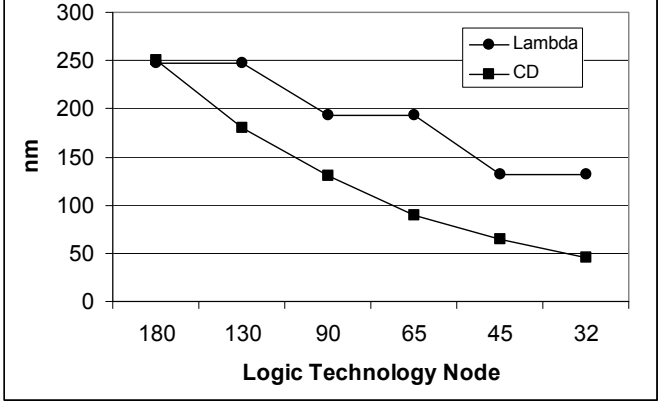


FIGURE 1. FEATURE SIZE VERSUS ILLUMINATION WAVELENGTH FOR RECENT LOGIC TECHNOLOGY NODES.

The relationship between lithography capability and design feature size requirement is given by the Rayleigh formula: $\mathbf{CD = k_1\ \lambda/NA}$, where k_1 is a fitting parameter related to difficulty, λ is the illumination wavelength, and NA is the numerical aperture.

The alternatives for reducing CD are clear: operate at a lower k_1 value (higher difficulty), use a shorter illumination wavelength, or use a higher NA. The wavelengths are limited by physics; state-of-the-art scanners use excimer lasers at 248nm or 193nm, or extend the effective wavelength to 132nm by using a combination of 193nm and immersion optics.

Each decrease in λ has come with a significant increase in capital and operating costs. Coupled with increasing NA, stepper costs have risen from ~$1M in 1986 to over $25M in 2005.

The net result of the rapid decrease in CD has been a decrease in k_1 from approximately 0.7 at the 250nm node to less than 0.4 at the 45nm node.

This decrease in k_1 has required a tremendous amount of engineering work in order to continue patterning the layouts coming from circuit designers. The effort includes software techniques such as optical proximity correction (OPC) applied to the design database prior to mask making. New mask types, such as attenuated-phase-shift or alternating-phase-shift, add complexity and cost to the mask-making process. Anti-reflective coatings (ARC) and chemically amplified resists are used in the wafer fab to improve contrast.

In spite of this effort, on many fronts, there are still yield problems linked to pattern fidelity. Numerous EDA start-ups have appeared to provide tools for finding and fixing "hot spots" in the layout. Unfortunately, the fix success rate is less than 100% in many cases.

DESIGN STYLE

According to Morris Chang of TSMC, "deeper and broader relationships with customers are needed, covering both design and technology engineering to allow for increasing demands for product-cost performance and reduced time-to-market."[2]

For a given set of design rules published by a technology development group, different design groups can end up with designs that have unique signatures. Even though every design passes the binary geometric design rule checks (DRC), there are still differences in the yield of good chips. These differences in yield can be traced to design style.

One way of considering design style is to look at the shapes used during physical design. This was described by Bill Arnold of ASML during the 32nm short course at IEDM 2006.[3] There is a range of styles, from random 2D shapes with bends and extra corners used for random logic, to highly structured 1D line shapes used for NAND FLASH memories. Figure 2 shows the trend in k_1 values versus logic node, including "practical limits" for 1D and 2D patterns. The graph clearly suggested that for a given k_1 value, 1D patterns have more manufacturability margin than 2D shapes. For 32nm logic, even an immersion scanner with an NA of 1.35 will not give a k_1 above the 2D practical limit.

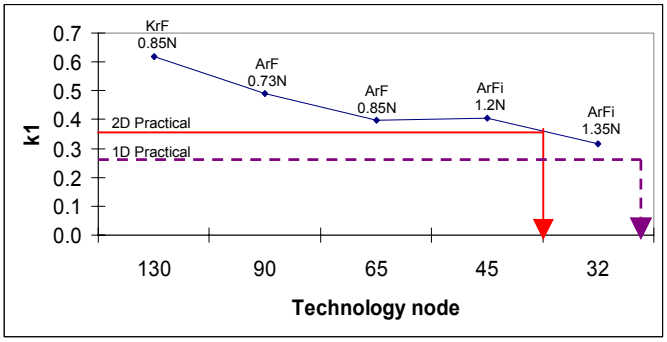
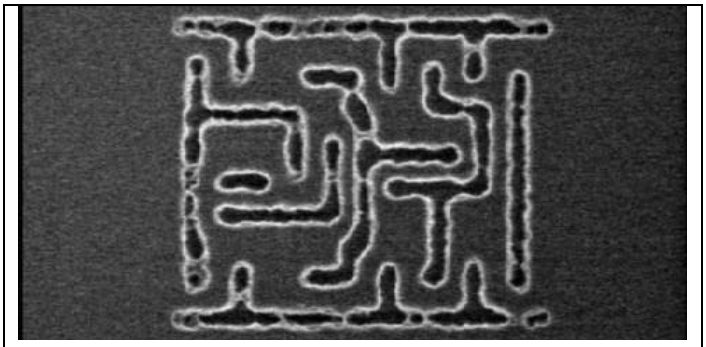


FIGURE 2. K1 TREND INCLUDING "PRACTICAL LIMITS" FOR 1D AND 2D PATTERNS.

Restricted design rules or radical design restrictions (RDRs) are a start in the direction of making design patterns more easily manufactured.[4, 5] Just as memory makers have used 1D grating patterns for many years to get tighter pitches for a given lithography equipment set, logic designers are looking more and more at 1D design styles.[6] Random logic does not equate to random layout any longer.

Several design styles were evaluated on a recent 45nm testchip.[7] The styles included traditional 2D layout, restricted layout with bends, and 1D layout with gaps. Figure 3 shows examples of these three styles.



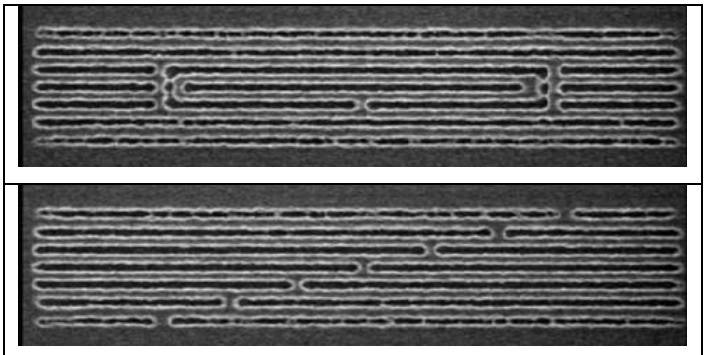


FIGURE 3. TRADITIONAL 2D, 1D WITH BENDS, 1D DESIGN STYLES.

The width/space rules for each style in Figure 3 are 65/65nm for the 45nm technology node. The 2D style has many problems, even with calibrated OPC. The 1D style with bends, using the same rules, has problems in the bends. The 1D style with only gaps has problems on the outer edge (top and bottom) lines, but the interior lines have good pattern fidelity.

From Figure 3, it's clear that although all three styles have the same k_1 of 0.31, there is a significant difference in the quality of the pattern results. It seems reasonable that another factor will be required to help assess true photolithography resolution.

The images in Figure 3 were created with an ASML XT 1400 scanner with annular illumination and NA=0.93. Further improvement for the pure 1D pattern could be achieved using dipole illumination and polarization. This illustrates that another factor is needed besides k_1 to represent the true capability of a photolithography system.

COST

Considering figures 2 and 3, there is a tradeoff between scanner NA and layout design style. Higher NA, especially with the addition of immersion for effective NA > 0.93, comes at a higher cost. In the past, the delta cost was more than offset by the reduction in area as a design moved from node to node. This improvement in chip cost is no longer guaranteed, as yield can be seriously impacted by systematic defects from litho hot spots. Unfortunately, not all hot spots can be corrected for any given random 2D layout.[8]

As shown in Figure 2, 1.2NA immersion scanners can be used at the 45nm node with some margin to the 2D practical limit. However, some wafer fabs are considering the 1D design style to allow use of 0.93NA dry scanners. This is based on memory experience and/or the desire to extend current litho capital equipment by an extra ½ or full node.

At the 32nm node, single exposure with 1.35NA immersion scanners would be at a k_1 value below the 2D practical limit. Clearly, either 1D patterns or a change in lithography will be required. The most likely litho change is a move to double exposure or double patterning.[2] This could be done with existing scanners, allowing wafer fabs to build prototype volumes at 32nm without investing in new litho capital equipment. The pattern splitting would be greatly simplified with more 1D patterns compared to traditional 2D patterns. Since not all mask levels would require double patterning, the overall chip litho cost should be lower at 32nm.

CONCLUSIONS

The cost roadmap for future technology nodes will not be as clear as it has been up to the 65nm node. New design styles will improve manufacturability at 45nm. These will be coupled with new litho approaches for 32nm.

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