Low k_1 Logic Design using Gridded Design Rules

Michael C. Smayling[a], Hua-yu Liu[b], Lynn Cai[b]
[a]Tela Innovations, Inc., 655 Technology Pkwy, Suite 150, Campbell, CA, USA 95008
[b]ASML Brion Technologies, 4211 Burton Dr., Santa Clara, CA USA 95054

ABSTRACT

Dimensions for 32nm generation logic are expected to be ~45nm. Even with high NA scanners, the k_1 factor is below 0.32. Gridded-design-rules (GDR) are a form of restricted design rules (RDR) and have a number of benefits from design through fabrication. The combination of rules and topologies can be verified during logic technology development, much as is done with memories. Topologies which have been preverified can be used to implement random logic functions with "hotspot" prevention that is virtually context-independent. Mask data preparation is simplified with less aggressive OPC, resulting in shorter fracturing, writing, and inspection times. In the wafer fab, photolithography, etch, and CMP are more controllable because of the grating-like patterns. Tela Canvas™ GDR layout was found to give smaller area cells than a conventional 2D layout style. Variability and context independence were also improved.

Keywords: Low k_1, gridded design rules, restricted design rules, context dependent hotspots

1. INTRODUCTION

The semiconductor industry has benefited from the continual improvement of photolithography resolution for the past 50 years. This has allowed integrated circuit designs to shrink from dimensions measured in mils to dimensions measured in nanometers. Until this decade, the exposure equipment resolution improvement with each technology node kept the k_1 value above 0.6, where k_1 is the fitting factor in the Rayleigh equation $CD = k_1 \lambda/NA$.

Recently, k_1 has been decreasing with each logic technology node as shown in Figure 1. To maintain pattern fidelity at k_1 values below ~0.6, optical proximity correction (OPC) and other resolution enhancement techniques (RET) have been introduced.

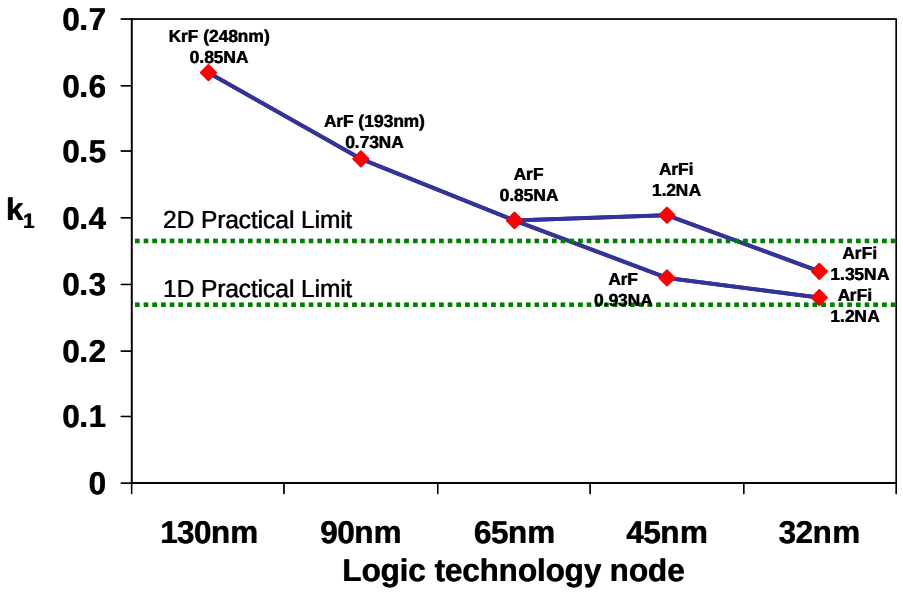

Fig. 1. k_1 trend for recent logic technology nodes. 1D and 2D practical limits are from [1].

As k_1 decreases, "practical limits" are imposed by the design style [1]. 2D refers to physical layouts with bent polygons. 1D refers to a layout style with parallel straight lines looking much like a grating pattern. The 1D lines can be in a vertical or horizontal direction, with gaps as needed to implement circuit functions. Because of the higher spatial resolution required, bends or corners in the 2D patterns are the limiting factors. Extensive efforts are being made to define "restricted design rules" which allow bends but with constraints on widths or spacings [2, 3]. A 1D layout style with further requirements for keeping lines on a regular grid permit using a simplified set of design rules described as "gridded design rules" [4].

2. GDR DESIGN SPACE HOTSPOT STUDY

2.1 Design space definition

The simplified GDRs used to create logic functions permit studying printability and ultimately optimizing design rules to minimize yield-killing hotspots. For this study, metal-1 pitch and end-gaps were the two variables chosen to cover the design space. Pitches ranged from 126nm to 140nm in 2nm increments. For each pitch, the line width and space were selected as the closest even value to being half of the pitch. For example, 126 = 64 + 62, 128 = 64 + 64, *etc*. The end gaps ranged from 62 to 80nm in 2nm increments. The complete matrix of 80 cells was generated using Tela software tools in two hours. A comparison to 2D layouts was not attempted because of the excessive time needed to create 80 cells using a conventional design style and rules.

2.2 Lithography simulations and analysis

The GDS file with the layout matrix was first run through the ASML Brion OPC software running on a Tachyon 2.0. Aerial images were simulated on a Tachyon 2.0 using the OPC output across a process window of ±100nm for focus, ±5% for the exposure dose. The 6% attenuated phase-shift mask was set as clear-geometry for the typical case of damascene copper for metal-1. The illuminator was set to annular, with an NA of 1.2, and sigma inner/outer of 0.4 and 0.85 respectively. Hotspot analysis was done on a Tachyon 2.0 using a bridging criterion of 59nm. For reference, a conventional layout-style cell with 140nm metal-1 pitch was run through the same simulation and analysis flow.

2.3 Results and discussion

The bridging hotspot counts for the 80 cells in the design space are shown in Figure 2.

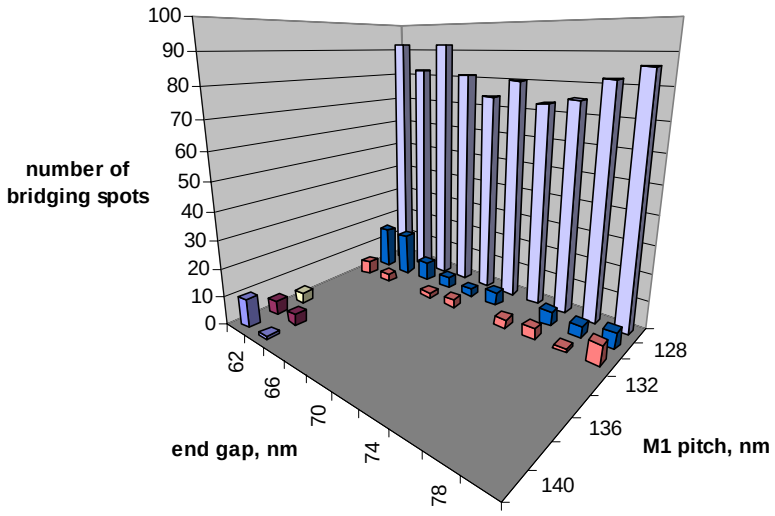

Fig. 2. Bridging hotspots for the metal-1 GDR design space

The bridging hotspots at pitches below 134nm were between adjacent lines. The bridging at pitches greater than 136nm was across the end-gaps, caused by the wide lines with relatively small end-gaps. There is clearly a large portion of the design space with **no** bridging hotspots. Note that the 2D style reference design with 140nm metal-1 pitch had **4** hotspots even with a relaxed bridging criterion of 56nm.

"Recommended" rules for the 2D style should give no hotspots but at a 10-15% area penalty compared to the standard design rules. In contrast, the Tela Canvas™ GDR layout style can give a no-hotspot result with an area savings of ~5%. This is a significant advantage for the GDR layout style, since the improvement in cell area can be extended to an area savings at the block and chip level. Further area improvements are expected for the GDR layout style once the scanner illumination is optimized for the limited set of patterns needed to create all SOC circuit functions.

For the 126nm metal-1 pitch layout with 70nm end-gap, the process window was evaluated using two different illuminator settings. Figure 3 shows that no hotspots were found at nominal exposure dose over a focus range of ±100nm for annular illumination. However, the dose range was fairly narrow, only ±3% at nominal focus. This is still an interesting result, given that it is at a pitch that is 10% smaller than the 2D standard of 140nm. The 10% smaller metal-1 pitch translates directly into a 10% reduction in standard cell height / area.

	df=-100	df=-75	df=-50	df=-25	df=0	df=25	df=50	df=75	df=100	
dd=9%	51	37	18	12	10	10	10	12	20	Bridging
dd=6%	3	2	1	1	1	1	1	1	1	
dd=3%	0	0	0	0	0	0	0	0	0	
dd=0%	0	0	0	0	0	0	0	0	0	
dd=-3%	53	7	0	0	0	0	0	0	3	
dd=-6%	55	51	45	25	12	11	19	47	48	Necking
dd=-9%	57	53	50	50	51	52	50	50	50	

Fig. 3. Number of metal-1 hotspots for annular illumination.

The same cell was simulated using quadrapole or "c-quad" illumination available using the Quasar™ system on an ASML scanner. As shown in Figure 4, the same ±100nm focus range was found at nominal dose. However, at nominal focus, the dose range increased significantly to +9/-6% without any hotspots. Given that bridging is more linked to yield problems than necking, at least for 1D patterns, the process window is good for both dose and focus.

	df=-100	df=-75	df=-50	df=-25	df=0	df=25	df=50	df=75	df=100	
dd=9%	14	3	0	0	0	0	0	0	0	Bridging
dd=6%	0	0	0	0	0	0	0	0	0	
dd=3%	0	0	0	0	0	0	0	0	0	
dd=0%	0	0	0	0	0	0	0	0	0	
dd=-3%	9	1	0	0	0	0	0	0	0	
dd=-6%	55	38	6	1	0	0	1	4	32	Necking
dd=-9%	59	54	51	50	48	51	51	50	50	

Fig. 4. Number of metal-1 hotspots for c-quad illumination.

Use of advanced illumination like quadrapole and dipole has been common in commodity memories for several generations. It is likely that these will be used for logic once the 1D GDR layout style becomes more widespread. The improvement in process window demonstrated by this study is significant and should influence the choice of layout style. It is expected that further improvement in process window can be achieved by further refinement of the illumination conditions.

3. REDUCED GATE CD VARIABILITY USING GDR

The single most important process factor impacting chip frequency and leakage current distributions is the gate electrode width in the channel region [5, 6, 7]. Gate CD control involves several sources of variability, including wafer-to-wafer, within-wafer, and within-die variability. Both the exposure and etch steps in the photolithography sequence impact the final CD.

Using integrated metrology and APC, each wafer's average CD can be controlled by adjusting the trim part of the etch process [8]. Within-wafer variability is typically controlled by reactant flow, chamber pressure, electrode power, and chuck bias. Within-die variability, caused by pattern-dependent micro-loading, can be controlled but at the expense of within-wafer variability.

Exposure uniformity is primarily impacted by illumination dose and focus. These factors are controlled within a "process window" validated by printing test wafers using an "FEM" (focus-exposure matrix). Modern scanners control dose and focus on a shot-by-shot basis.

3.1 Variability experiment design

Six typical logic cells were chosen for the evaluation. Three cells had fairly regular gate patterns in the conventional 2D design style, while the other three had relatively complex patterns. The GDR versions of these cells had extremely regular gate patterns in all six cases. These six cells are representative of the majority of logic functions used for typical blocks placed into SOCs.

For each of the six cells, four layout cases were created. These cases are summarized in Table 1 below. Each logic cell had at least two placements of the cell within a larger array of cells surrounding it on the top, bottom, left, and right. The larger cells had three rows and four columns in the arrays, while the smaller cells had three rows and up to 20 columns in individual arrays. Although all of the gates in each array were run through OPC and aerial image simulation, only cells in the middle of the array were analyzed for gate CD over diffusion. The number of transistors in each array was kept approximately the same to give similar statistical populations.

Table 1. Cell environments for the gate CD variability experiment.

Case	Surrounding cell
1. 2D conventional layout	Itself
2. 2D conventional layout	Complex pattern cell
3. 2D conventional layout	Simple pattern cell
4. GDR layout	Itself

The 24 combinations of cell type and environment were placed in a 6 x 4 matrix. Figure 5 shows the matrix, with 6 rows of arrays, each row having one functional cell type. The columns are each of the cases listed in Table 1, with case 1 on the left and case 4 on the right.

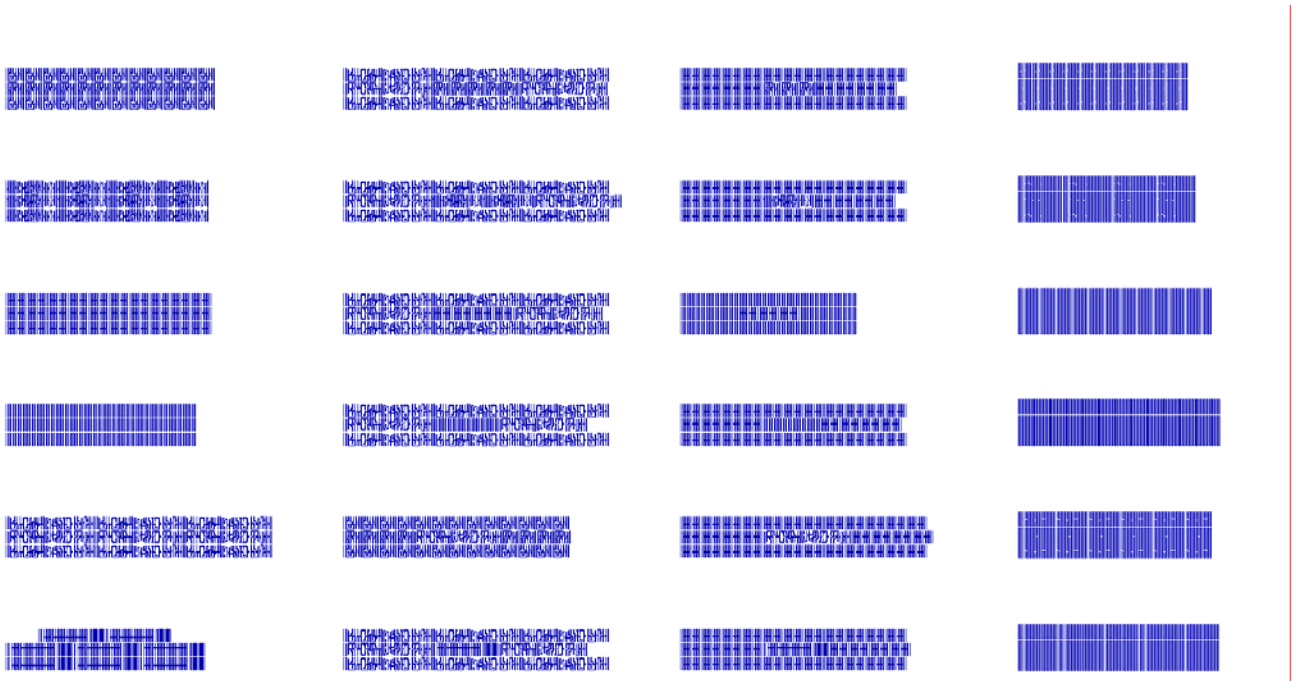

Fig. 5. Gate patterns for six different logic cells in different environments.

3.2 Variability experiment simulations and analysis

Simulations were done within a process window to determine the distribution of gate CD as a function of different design styles. Focus was varied over a range of ±100nm, while a ±5% range was used for the exposure dose. The GDS file with the layout matrix was first run through the ASML Brion OPC software running on a Tachyon 2.0. Aerial images were simulated on a Tachyon 2.0 using the OPC output across the process window. The 6% attenuated phase-shift mask had dark-geometry for the gate pattern. The illuminator was set to annular, with an NA of 1.2, and sigma inner/outer of 0.4 and 0.85 respectively. CD analysis was done on the output aerial image using Cell Designer from Sequoia Design Systems, based on splitting the transistors into many parallel stripes and then measuring the gate CD for each stripe.

Table 2 summarizes the results of the CD's measured from the nominal dose and focus aerial images. The coefficient of variation (standard deviation divided by the mean) for gate CD's is shown for each of the logic functions and different design style or environment. For the 2D design styles, the CoV was consistent for each logic function, but showed large differences between logic functions. The more complex cells with more 2D patterns had nearly 20 times larger CoV compared to 2D cells with more simple patterns. In all cases, the 1D cells not only had much lower CD CoV, but they all had a CoV which was nearly independent of the logic function.

Table 2. Coefficient of variation for gate CD for each cell types and environment.

Function	Case 1	Case 2	Case 3	Case 4
F	7.0%	7.0%	7.0%	0.2%
E	1.2%	1.1%	1.2%	0.3%
D	0.9%	0.8%	0.9%	0.4%
C	0.9%	0.8%	1.0%	0.0%
B	16.0%	16.2%	16.3%	0.0%
A	7.2%	7.2%	7.1%	0.4%

The variability of CD CoV for a GDR 1D cell with different surroundings was studied by looking at the CD's for each location of functional cell "E" in an array of cells. Figure 6 shows the array of cells used, giving multiple corner, edge, and central cells. Note that the middle row of cells is reflected in the y direction, as is normally done in blocks of standard cells, so that the power supply rails can be shared.

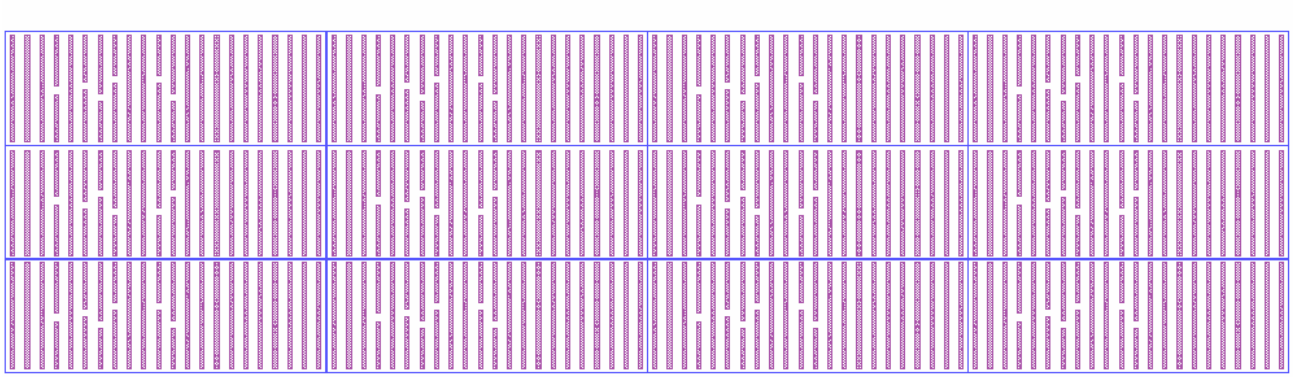

Fig. 6. Gate pattern for one cell in 12 different locations.

The CoV for each cell shown in Figure 6 is listed in Table 3. The data show that the cell gate CD uniformity was very good, independent of location within the array. These are identical to the results in Table 2, which included only results from the center two cells in the middle row.

Table 3. Coefficient of variation for gate CD for each cell in the Figure 4 array.

0.2%	0.2%	0.3%	0.4%
0.2%	0.3%	0.3%	0.3%
0.1%	0.3%	0.3%	0.3%

A larger array of cells was simulated to see if the Tela 1D style was uniform across a large area, or there was some form of context dependence. 5x6, 7x8, and 9x10 arrays were tested using the same design and simulation flow. The results for the 9x10 array of cells is tabulated in Table 4. The CoV ranges from 0.1% to 0.4% across the array, with no pattern in the variation. The arrays included extra features around the edges to maintain pattern density.

Table 4. Coefficient of variation for gate CD for each cell in a 9x10 array.

0.3%	0.4%	0.3%	0.4%	0.3%	0.3%	0.4%	0.3%	0.3%	0.3%
0.3%	0.3%	0.3%	0.3%	0.3%	0.3%	0.4%	0.2%	0.3%	0.3%
0.3%	0.3%	0.3%	0.3%	0.3%	0.4%	0.3%	0.2%	0.3%	0.3%
0.3%	0.4%	0.4%	0.2%	0.4%	0.2%	0.4%	0.3%	0.4%	0.4%
0.4%	0.4%	0.4%	0.2%	0.3%	0.2%	0.4%	0.3%	0.3%	0.3%
0.2%	0.3%	0.3%	0.3%	0.3%	0.3%	0.3%	0.1%	0.3%	0.4%
0.3%	0.4%	0.2%	0.2%	0.3%	0.3%	0.4%	0.3%	0.4%	0.3%
0.3%	0.3%	0.3%	0.3%	0.3%	0.1%	0.4%	0.2%	0.3%	0.3%
0.3%	0.3%	0.4%	0.3%	0.3%	0.4%	0.4%	0.2%	0.4%	0.3%

4. CONCLUSIONS

Test cells laid out using gridded design rules and the Tela Canvas 1D style have been shown to provide better yield-ability, smaller area, and better uniformity than test cells drawn with a conventional 2D layout style. Complex logic function layouts had hotspots even using approved layout rules, resulting in either yield loss or costly rework of final chip layout. Variability in gate CD was much less for cells drawn using GDR and the Tela Canvas, with the range reduced by 4x to 16x depending on the conventional layout functionality. GDR cells had gate CD variability which was essentially independent of logic function. Finally, GDR cells within a small buffer had nearly context-independent gate CD variability, eliminating the need for post place-and-route layout adjustments.

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